Exhibit E
Part 2 of 2

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	46	of	47	Attorney Docket Number	***129980-5023-US01***

	863.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.
	864.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.
	865.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Complaint For Patent Infringement, filed Sep. 22, 2009 in 10 pages. cited by other.
	866.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's Complaint for Patent Infringement, filed Nov. 12, 2009 in 6 pages. cited by other.
	867.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's First Amended Complaint for Patent Infringement, filed Feb. 11, 2010 in 9 pages. cited by other.
	868.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Notice of Motion and Motion for Stay Pending Reexaminations and Interference Proceeding Regarding the Patents-In-Suit; Memorandum of Points and Authorities in Support Thereof, filed Apr. 21, 2010 in 28 pages. cited by other.
	869.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Plaintiff Netlist Inc's Opposition to Defendant Inphi Corporation's Motion for Stay Pending Reexaminations and Interference Proceedings Regarding the Patents-In-Suit, filed May 3, 2010 in 23 pages. cited by other.
	870.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Plaintiff Netlist, Inc's First Amended Complaint For Patent Infringement, filed Dec. 23, 2009 in 8 pages. cited by other.
	871.	US District Court Civil Docket; Netlist Inc. v. Google Inc.; 4:09cv5718; Date filed Dec. 4, 2009. In 10 pages. cited by other.
	872.	U.S. Court of Appeals for the Federal Circuit, Decision on Appeal for Reexamination Control No. 95/001,381, filed November 13, 2015, 14 pages
	873.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Corrected Joint Claim

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	*16/695,020*
				Filing Date	*November 25, 2019*
				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*TBD*
Sheet	47	of	47	Attorney Docket Number	*129980-5023-US01*

	874.	Construction and Prehearing Statement Pursuant to Patent L.R. 4-3, including Exhibit A, filed August 27, 2014, 28 pages.
	875.	Notice of Allowance, U.S. Pat. App. No. 12/504,131, February 12, 2013, 52 pages
	876.	Non-Final Office Action, U.S. Pat. App. No. 12/761,179, September 13, 2012, 20 pages
	877.	Response to non-final office action dated September 13, 2012 for U.S. Patent Application No. 12/761,179, filed March 13, 2013, 16 pages
	878.	Notice of Allowance, U.S. Pat. App. No. 12/761,179, July 11, 2013, 37 pages
	879.	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042 filed November 1, 2011, 42 pages
	880.	Response to Non-Final Office Action dated January 2, 2014 for U.S. Pat. App. No. 13/287,042, filed April 2, 2014, 12 pages
	881.	Non-final office action, U.S. Patent Application No. 13/288,850, October 14, 2013, 24 pages
	882.	Response to non-final office action dated October 14, 2013 for U.S. Patent Application No. 13/288,850, filed January 14, 2014, 15 pages
	883.	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages
	884.	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages
	885.	Non-Final Office Action, U.S. Pat. App. No. 13/412,243, January 2, 2014, 20 pages
	886.	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages
	887.	Office Action mailed April 2, 2014, for Japanese Patent Application No. JP 2012-520662 and English translation thereof, 7 pages
	888.	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.
	889.	International Preliminary Report on Patentability for International Application No. PCT/US2010/040826, date of mailing November 28, 2011 (NETL.048VPC) in 34 pages.
	890.	International Search Report and Written Opinion for Related Application No. PCT/US2010/040826, mailed on September 27, 2010, in 15 pages.
	891.	International Search Report and Written Opinion, PCT Application No. PCT/US2011/059209, January 31, 2013

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

A 6.4-Gb/s near-ground single-ended transceiver for dual-**rank** **DIMM** memory interface systems

M Bucher, RT Kollipara, B Su... - IEEE Journal of Solid ..., 2013 - ieeexplore.ieee.org

... a point-to-two point configuration for a dual-**rank** system [4]. Additional **ranks** could be ... et al.: 6.4-GB/S NEAR-GROUND SINGLE-ENDED TRANSCEIVER FOR DUAL-**RANK** **DIMM** MEMORY INTERFACE ... goal was to keep this under 10 nS or comparable to the **CAS** **latency** of the ...

☆ 99 Cited by 20 Related articles All 3 versions

A 1.0-ns/1.0-V delay-locked loop with racing mode and countered **CAS** **latency** controller for DRAM interfaces

HW Lee, H Choi, BJ Shin, KH Kim... - IEEE journal of solid ..., 2012 - ieeexplore.ieee.org

... on 667-DDR2 by 39% when the server is in idle state [1]. **DIMM** based DDR3 ... al., "A 1.6-Gb/s/pin double data rate SDRAM with wave- pipelined **CAS** **latency** control," IEEE ... loop using power noise management technique with unregulated power supply for pseudo-**rank** DRAM in ...

☆ 99 Cited by 32 Related articles All 6 versions

A DDR2 controller for BEE3

C Thacker - Microsoft Research, 2009 - atitla.ac.upc.edu

... which reduce the loading on the address and control lines at the expense of an extra cycle of **CAS** **latency** ... Each **DIMM** consists of two **ranks**, for a total of four **ranks** per controller ... Note that the controller uses location 0 in **rank** 1 during calibration, so user logic should not make ...

☆ 99 Cited by 13 Related articles »

Fully-buffered **DIMM** memory architectures: Understanding mechanisms, overheads and scaling

B Ganesh, A Jaleel, D Wang... - 2007 IEEE 13th ..., 2007 - ieeexplore.ieee.org

... DD0 RAS DD3 **CAS** DD1 DD2 D2 D1 D3 Southbound bus ... Typically, single-**rank** configurations have higher **latencies** due to insufficient number of memory banks to distribute requests to ... Adding more **ranks** in these system helps reduce the **DIMM**-based queueing delays ...

☆ 99 Cited by 104 Related articles All 13 versions »

Analysis of Memory Performance: Mixed **Rank** Performance Across Microarchitectures

M Bouache, JL Glover, J Boukhobza - International Conference on High ..., 2016 - Springer

... section, we are giving a background about the memory architecture, **ranking**, different types ... QRDIMMs (Quad **Ranked** **DIMMs**) are generally not recommended for best performance ... memory RAS (Row Access Select) modes [12]: Independent Channel Mode, **Rank** Sparing Mode ...

☆ 99 Cited by 1 Related articles All 3 versions

DECO: **DIMM** controller efficient for ECC operations

W Jang - Electronics Letters, 2014 - IET

... **DIMM**. **DIMMs** consist of two **ranks** and each **rank** includes nine syn- chronous dynamic random access memories (SDRAMs). Reversely ... command. The **DIMM** generates 9 byte ECC words after the **CAS** **latency** (CL) from the first **CAS** command ...

☆ 99 Cited by 1 Related articles All 7 versions »

Minimizing DRAM **rank** switching overhead for improved timing bounds and performance

L Ecco, A Kostrzewa, R Ernst - 2016 28th Euromicro ..., 2016 - ieeexplore.ieee.org

... If both **CAS** commands are of the same type, the cal- culations are simpler: for tRDRD dr, the ... tRTRS = 2 cycles, which, as described in Table II, is only valid for a dual-**rank** module with a ... In [15], [20], a TDM schedule is used to alternate be- tween the **ranks** and, consequently, the ...

☆ 99 Cited by 15 Related articles

PRET DRAM controller: Bank privatization for predictability and temporal isolation

J Reineke, I Liu, HD Patel, S Kim... - 2011 Proceedings of the ..., 2011 - ieeexplore.ieee.org

... right side of Fig- ure 1 depicts a high-level view of the dual-**ranked** dual in ... sharing of I/O mechanisms within a device, consec- utive accesses to the same **rank** are more ... We later exploit this subtle difference by restricting consecutive accesses to different **ranks** to achieve more ...

☆ 99 Cited by 220 Related articles All 13 versions »

Decoupled **DIMM**: building high-bandwidth memory system using low-speed DRAM devices

H Zheng, J Lin, Z Zhang, Z Zhu - ACM SIGARCH Computer Architecture ..., 2009 - dl.acm.org

... which for DDR3 systems includes BA0-BA2 (banks address), A0-A13 (row/column address), RAS (Row Address Strobe), **CAS** (Column Address ... hit **latency** MSHR entries Inst:8, Data:32, L2:64 Memory 4/2/1-channels, 2-**DIMMs**/channel, 2-**ranks**/**DIMM**, 8-banks/**rank**, 9-devices ...

☆ 99 Cited by 91 Related articles All 13 versions

Duo: Exposing on-chip redundancy to **rank**-level ecc for high reliability

SL Gong, J Kim, S Lym, M Sullivan... - ... Symposium on High ..., 2018 - ieeexplore.ieee.org

... write **latency** = 10ns ... to maintain the 12.5% redundancy level; only a single ×4 redundant device will be available with a 32-bit wide **rank** and a ... This poses a challenge in achieving high reliability as seen today with ×8 DDR4-generation **ranks**, which cannot provide true SDDC ...

☆ 99 Cited by 10 Related articles All 5 versions

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	190	CS with buffer with RANK	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:25
L8	5,794	CAS with latency	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:35
L9	2,116	CAS with latency with memory	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:35
L10	1,704	CAS adj latency with memory	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:35
L11	221	CAS adj latency with memory with (DIMM module rank)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:35
L12	503	grundy.in.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:41
L13	1,171	CS with dimm	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:43
L14	18,887	CS with rank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:47
L15	95	CS with rank same burst	US-PGPUB;	OR	ON	2021/03/25 01:47

			USPAT; EPO; IBM_TDB			
L16	130	(US-4218740-$ | US-4249253-$ | US-4368515-$ | US-4392212-$ | US-4571676-$ | US-4592011-$ | US-4633429-$ | US-4670748-$ | US-4706214-$ | US-4739473-$ | US-4866603-$ | US-4958322-$ | US-4961172-$ | US-4961204-$ | US-4980850-$ | US-5060188-$ | US-5247643-$ | US-5272664-$ | US-5313624-$ | US-5345412-$ | US-5357478-$ | US-5388072-$ | US-5388240-$ | US-5392252-$ | US-5426753-$ | US-5463590-$ | US-5483497-$ | US-5485589-$ | US-5495435-$ | US-5513135-$ | US-5532954-$ | US-5537584-$ | US-5541448-$ | US-5559970-$ | US-5572691-$ | US-5581498-$ | US-5590071-$ | US-5602999-$ | US-5617559-$ | US-5630096-$ | US-5638534-$ | US-5649159-$ | US-5655153-$ | US-5699542-$ | US-5702984-$ | US-5703826-$ | US-5717851-$ | US-5724604-$ | US-5729716-$ | US-5745914-$ | US-5764590-$ | US-5784705-$ | US-5802395-$ | US-5802541-$ | US-5805520-$ | US-5822251-$ | US-5905401-$ | US-5909388-$ | US-5926827-$ | US-5926839-$ | US-5953215-$ | US-5953280-$ | US-5958025-$ | US-5959930-$ | US-5963464-$ | US-5966736-$ | US-5973392-$ | US-5974493-$ | US-6011710-$ | US-6018787-$ | US-6044032-$ | US-6061754-$ | US-6070217-$ | US-6070227-$ | US-6097652-$ | US-6108745-$ | US-6115278-$ | US-6134638-$ | US-6141245-$ | US-6151271-$ | US-6154418-$ | US-6154419-$ | US-6173357-$ | US-6185654-$ | US-6188641-$ | US-6205516-$ | US-6209074-$ | US-6223650-$ | US-6226709-$ | US-6226736-$ | US-6233650-$ | US-6247088-$ | US-6260127-$ | US-6262938-$ | US-6317352-$ | US-6349051-$ | US-6381140-$ | US-6400637-$ | US-	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 01:50

		6408356-$ | US-6414868-$ | US-6415374-$ | US-6438062-$ | US-6446158-$ | US-6446184-$ | US-6453381-$ | US-6470417-$ | US-6480439-$ | US-6487102-$ | US-6502161-$ | US-6518794-$ | US-6526473-$ | US-6530007-$ | US-6530033-$ | US-6546476-$ | US-6553449-$ | US-6553450-$ | US-6618320-$ | US-6618791-$ | US-6621496-$ | US-6625081-$ | US-6625687-$ | US-6636446-$ | US-6636935-$ | US-6646949-$ | US-6658509-$ | US-6674684-$ | US-6681301-$ | US-6683372-$ | US-6697888-$ | US-6704910-$).DID.				
L17	27,800	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:16
L18	0	(G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.) with CAS with latency	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:19
L19	1,288	(G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.) and CAS with latency	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:19
L20	80	(G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.) and CAS with latency same rank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:19
L21	2,861	CS with rank and @pd<="20060101"	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:39
L22	99	CS with rank with memory and @pd<="20060101"	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/25 02:39
S1	18,362	G06F3/0683.cpc. G06F3/0604.cpc. G06F3/0655.cpc.	US-PGPUB; USPAT;	OR	ON	2021/03/17 11:52

			EPO; IBM_TDB			
S2	31,786	memory adj bank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 11:57
S3	579	S1 and S2	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 11:57
S4	5,003	memory adj bank with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 20:41
S5	416	memory adj bank with controller with (switch mux multiplexer)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 20:57
S6	502	grundy.in.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 21:03
S7	27	DIMM with memory with controller with MUX	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/17 21:47
S8	107	RAM with memory with controller with MUX	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:23
S9	1	RAM with tiles same memory with controller same mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:42
S10	1	RAM with tiles same memory with controller same switch	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:44

S11	63	RAM with bank same memory with controller same switch	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:52
S12	4,598,109	memory controller with memory adj bank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:57
S13	2,379	memory adj controller with memory adj bank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:58
S14	221	memory adj controller with memory adj bank same (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 00:58
S15	621	memory adj controller with RAM same (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:12
S16	0	"tile.clm" and "bansal.xa"	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:24
S17	0	tile and bansal.xa.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:24
S18	8	tile and bansal.xp.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:24
S19	4,598,512	memory controller with (MUX Switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:33
S20	220	memory adj controller with (MUX Switch) with RAM	US-PGPUB; USPAT;	OR	ON	2021/03/18 01:33

			EPO; IBM_TDB			
S21	103	memory adj controller with (MUX Switch) with DIMM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:44
S22	30,028	(MUX switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:59
S23	352	(MUX switch) with banks with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 01:59
S24	30,028	(MUX switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 02:11
S25	426	memory adj controller same (MUX switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 02:12
S26	25	power adj island and (MUX switch) with RAM	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 02:21
S27	64	DIMM with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 03:07
S28	502	grundy.in.	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 10:33
S29	426	memory adj controller same RAM with (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 10:49

S30	4,750	controller same bank with (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 10:55
S31	5,010	parallel with memory with bank	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 11:10
S32	686	parallel with memory with bank and mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 11:10
S33	3,316	parallel with memory with bank and (mux switch$3)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 11:10
S34	226	parallel with RAM with bank and mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 17:58
S35	1	parallel with RAM with bank with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 17:58
S36	50	RAM with bank with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 17:58
S37	2,070	RAM with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 18:00
S38	209	RAM with mux with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 18:00
S39	36	DIMM with mux with controller	US-PGPUB; USPAT;	OR	ON	2021/03/18 18:00

			EPO; IBM_TDB			
S40	184	DIMM with switch with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/18 18:02
S41	336	pipelin$3 and bank with mux same controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:09
S42	556	controller with memory adj bank same (switch mux)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:17
S43	955	bank with select$3 with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:26
S44	43	rank with select$3 with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:49
S45	618	ram with select$3 with mux	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/19 03:53
S47	8	DIMM with mux with CS	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 17:51
S48	300	memory with mux with CS	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 17:55
S49	703	RAM with tiles and (mux switch)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:36

S50	121	RAM with tiles same2 (mux switch)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:36
S51	48	Die with mux with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:39
S52	209	RAM with mux with controller	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:42
S53	369	MRAM with compar$3 with flash	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 18:44
S54	5,539	(switch mux) with parallel with memory	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 21:46
S55	437	(switch mux) with parallel with memory with (die chip plane dimm)	US-PGPUB; USPAT; EPO; IBM_TDB	OR	ON	2021/03/23 21:47

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L23	13,642	G06F13/1673.cpc. G06F12/00.cpc. G06F13/00.cpc. G06F13/4243.cpc. G06F13/4282.cpc. G11C5/04.cpc. G11C7/1072.cpc. G11C15/00.cpc.	USPAT	OR	ON	2021/03/25 03:03
L24	114	burst.clm. and CAS.clm. and latency.clm.	USPAT	OR	ON	2021/03/25 03:04
L25	29	L23 and L24	USPAT	OR	ON	2021/03/25 03:04

3/25/2021 3:06:42 AM
C:\Users\gbansal\Documents\EAST\Workspaces\16695020.wsp

Electronically filed June 17, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. SOLOMON	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2139
Filed:	25-Nov-2019	Examiner:	BANSAL, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Mail Stop: Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is filed under 37 C.F.R. § 1.312 for the above identified patent application, and is filed after a Notice of Allowance dated March 30, 2020.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5023-US01).

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to ~~are configured to receive~~ respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices in one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the

other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an ~~additional~~ amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

2. (Original) The memory module of claim 1, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

3. (Currently Amended) The memory module of claim 1, wherein the [[first]] burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals.

4. (Currently Amended) The memory module of claim 1, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 64-bits or 72-bits wide and includes 16 or 18 memory devices configured in pairs~~, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device~~.

5. (Currently Amended) The memory module of claim 1, wherein the memory devices are organized in four ranks and the [[first]] set of input address and control signals include four chip select signals, one for each of the four ranks.

6. (Original) The memory module of claim 1, wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry.

7. (Original) The memory module of claim 1, wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.

8. (Currently Amended) The memory module of claim 1, wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred between the one of the plurality of N-bit wide ranks and the memory controller at the specified data rate.

9. (Original) The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

10. (Currently Amended) The memory module of claim 9, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of N-bit wide ranks is configured to receive or output a respective set of bits of the ~~first~~ burst of N-bit wide data signals on both edges of each of a respective set of data strobes.

11. (Currently Amended) The memory module of claim 1, wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths.

12. (Original) The memory module of claim 11, wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.

13. (Original) The memory module of claim 12, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

14. (Original) The memory module of claim 12, wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred through the data paths at the specified data rate.

15. (Original) The memory module of claim 12, wherein the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths.

REMARKS

This amendment is filed after the Notice of Allowance dated March 30, 2021, which allowed claims 1-15.

Claims 1, 3-5, 8, and 10-11 been amended to address minor issues of clarity. No new matter is added, and the amendments should not require additional search or examination.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: June 17, 2021

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

Phone: (650) 521-4828

Electronic Acknowledgement Receipt

EFS ID:	43010800
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5023-US01
Receipt Date:	17-JUN-2021
Filing Date:	25-NOV-2019
Time Stamp:	03:19:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5023-US01_312_Amendment.pdf	123602 2550b35eec548731fdccc473a1708c1fc2338f2c	yes	6

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Amendment after Notice of Allowance (Rule 312)	1	1
Claims	2	5
Abstract	6	6

Warnings:	
Information:	
Total Files Size (in bytes):	123602

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	16695020
Filing Date:	25-Nov-2019
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5023-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1200**

Electronic Acknowledgement Receipt

EFS ID:	43143194
Application Number:	16695020
International Application Number:	
Confirmation Number:	7514
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5023-US01
Receipt Date:	30-JUN-2021
Filing Date:	25-NOV-2019
Time Stamp:	21:36:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1200
RAM confirmation Number	E20216TL37170395
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	129980-5023-US01_Issue-Fee-Payment_2021-06-30.pdf	311477 2cec4f25f4f23fa9075404515a836ce46f670721	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30502 3020f0bcc9cbc4cd2290356da3453a24a02d5348	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	341979		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 03/30/2021
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Jamie J. Zheng	(Typed or printed name)
/Jamie J. Zheng/	(Signature)
2021-06-30	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/30/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 USCH Law, PC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☑ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☑ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 60-3916

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jamie J. Zheng/ Date 2021-06-30

Typed or printed name Jamie J. Zheng Registration No. 51167

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 03/30/2021

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 03/30/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

TITLE OF INVENTION: MEMORY MODULE WITH DATA BUFFERING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/30/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	11/25/2019	Jefferey C. Solomon	129980-5023-US01	7514

79141 7590 07/09/2021

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
07/09/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

Response to Rule 312 Communication	Application No.	Applicant(s)	
	16/695,020	Solomon et al.	
	Examiner	Art Unit	AIA (FITF) Status
	GURTEJ BANSAL	2139	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 17 June 2021 under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☑ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

OK TO ENTER: /G.B/

Electronically filed June 17, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. SOLOMON	Confirmation No.:	7514
Serial No.:	16/695,020	Art Unit:	2139
Filed:	25-Nov-2019	Examiner:	BANSAL, Gurtej
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	129980-5023-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Mail Stop: Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is filed under 37 C.F.R. § 1.312 for the above identified patent application, and is filed after a Notice of Allowance dated March 30, 2020.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5023-US01).

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	6	of	47	Attorney Docket Number	***129980-5023-US01***

Change(s) applied to document, /S.B./ 4/28/2021

	166.	7,007,175	2006-02-28	Chang et al.	
	167.	7,024,518	2006-04-04	Halbert et al.	
	168.	7,046,538	2006-05-16	Kinsley et al.	
	169.	7,047,361	2006-05-16	~~Phison Electronics Corp.~~	Chong et al.
	170.	7,054,179	2006-05-30	Cogdill et al.	
	171.	7,065,626	2006-06-20	Schumacher et al.	
	172.	7,072,231	2006-07-04	Pax	
	173.	7,073,041	2006-07-04	Dwyer et al.	
	174.	7,078,793	2006-07-18	Ruckerbauer et al.	
	175.	7,093,066	2006-08-15	Klein	
	176.	7,120,727	2006-10-10	Lee et al.	
	177.	7,124,260	2006-10-17	LaBerge et al.	
	178.	7,127,584	2006-10-24	Thompson et al.	
	179.	7,130,308	2006-10-31	Haddock et al.	
	180.	7,130,952	2006-10-31	Nanki et al.	
	181.	7,133,960	2006-11-07	Thompson et al.	
	182.	7,133,972	2006-11-07	Jeddeloh	
	183.	7,142,461	2006-11-28	Janzen	
	184.	7,149,841	2006-12-12	LaBerge	
	185.	7,167,967	2007-01-23	Bungo et al.	
	186.	7,181,591	2007-02-20	Tsai	
	187.	7,191,302	2007-03-13	Usami	
	188.	7,200,021	2007-04-03	Raghuram	
	189.	7,225,303	2007-05-29	Choi	
	190.	7,227,910	2007-06-05	Lipka	
	191.	7,254,036	2007-08-07	Pauley et al.	
	192.	7,266,639	2007-09-04	Raghuram	
	193.	7,272,709	2007-09-18	Zitlaw et al.	
	194.	7,281,079	2007-10-09	Bains et al.	
	195.	7,286,436	2007-10-23	Bhakta et al.	
	196.	7,289,386	2007-10-30	Bhakta et al.	
	197.	7,334,150	2008-02-19	Ruckerbauer et al.	
	198.	7,346,750	2008-03-18	Ishikawa	
	199.	7,356,639	2008-04-08	Perego et al.	

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	5	of	47	Attorney Docket Number	***129980-5023-US01***

Change(s) applied to document, /S.B./ 4/28/2021

	132.	6,705,877	2004-03-16	Li et al.	
	133.	6,717,855	2004-04-06	Underwood	
	134.	6,717,885	2004-04-06	Lai	
	135.	6,721,843	2004-04-13	~~Lexar Media Inc~~ Estakhri	
	136.	6,721,860	2004-04-13	Klein	
	137.	6,738,880	2004-05-18	Lai et al.	
	138.	6,742,098	2004-05-25	Halbert et al.	
	139.	6,747,887	2004-06-08	Halbert et al.	
	140.	6,754,797	2004-06-22	Wu et al.	
	141.	6,785,189	2004-08-31	Jacobs et al.	
	142.	6,788,592	2004-09-07	Nakata et al.	
	143.	6,807,125	2004-10-19	Coteus et al.	
	144.	6,807,650	2004-10-19	Lamb et al.	
	145.	6,813,196	2004-11-02	Park et al.	
	146.	6,832,284	2004-12-14	Perego et al.	
	147.	6,832,303	2004-12-14	Tanaka	
	148.	6,834,014	2004-12-21	Yoo et al.	
	149.	6,854,042	2005-02-08	Karabatsos	
	150.	6,880,094	2005-04-12	LaBerge	
	151.	6,889,304	2005-05-03	Perego et al.	
	152.	6,912,615	2005-06-28	Nicolai	
	153.	6,912,628	2005-06-28	Wicki et al.	
	154.	6,925,028	2005-08-02	Hosokawa et al.	
	155.	6,944,694	2005-09-13	Pax	
	156.	6,948,084	2005-09-20	Manapat et al	
	157.	6,950,366	2005-09-27	Lapidus et al.	
	158.	6,954,281	2005-10-11	Fukuda et al	
	159.	6,961,281	2005-11-01	Wong et al.	
	160.	6,981,089	2005-12-27	Dodd et al.	
	161.	6,982,892	2006-01-03	Lee et al.	
	162.	6,982,893	2006-01-03	Jakobs	
	163.	6,990,043	2006-01-24	Kuroda et al.	
	164.	6,996,686	2006-02-07	Doblar et al.	
	165.	7,007,130	2006-02-28	Holman	

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	3	of	47	Attorney Docket Number	***129980-5023-US01***

Change(s) applied to document, /S.B./ 4/28/2021

	64.	5,959,930	1999-09-28	Sakurai	
	65.	5,963,464	1999-10-05	Dell et al.	
	66.	5,966,736	1999-10-12	Gittinger et al.	
	67.	5,973,392	1999-10-26	Senba et al.	
	68.	5,974,493	1999-10-26	~~Mitsubishi Electric Corp~~	Okumura et al.
	69.	6,011,710	2000-01-04	Wiggers	
	70.	6,018,787	2000-01-25	Ip	
	71.	6,044,032	2000-03-28	Li	
	72.	6,061,754	2000-05-09	Cepulis	
	73.	6,070,217	2000-05-30	Connolly et al.	
	74.	6,070,227	2000-05-30	Rokicki	
	75.	6,097,652	2000-08-01	Roh	
	76.	6,108,745	2000-08-22	Gupta et al.	
	77.	6,115,278	2000-09-05	Deneroff et al.	
	78.	6,134,638	2000-10-17	Olarig et al.	
	79.	6,141,245	2000-10-31	Bertin	
	80.	6,151,271	2000-11-21	Lee	
	81.	6,154,418	2000-11-28	Li	
	82.	6,154,419	2000-11-28	Shakkarwar	
	83.	6,173,357	2011-01-09	Ju	
	84.	6,185,654	2001-02-06	Van Doren	
	85.	6,188,641	2001-02-13	Uchida	
	86.	6,205,516	2001-03-20	Usami	
	87.	6,209,074	2001-03-27	Dell et al.	
	88.	6,223,650	2001-05-15	Johnson	
	89.	6,226,709	2001-05-01	Goodwin et al.	
	90.	6,226,736	2001-05-01	Niot	
	91.	6,233,650	2001-05-15	Johnson et al.	
	92.	6,247,088	2001-06-12	Seo et al.	
	93.	6,260,127	2001-07-10	Olarig et al.	
	94.	6,262,938	2001-07-17	Lee	
	95.	6,317,352	2001-11-13	Halbert et al.	
	96.	6,349,051	2002-02-19	~~Micron Technology Inc~~	Klein
	97.	6,381,140	2002-04-30	Liao, Sheng-Chi	

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	2	of	47	Attorney Docket Number	***129980-5023-US01***

	31.	5,532,954	1996-07-02	Bechtolsheim et al.	
	32.	5,537,584	1996-07-16	Miyai et al.	
	33.	5,541,448	1996-07-30	Carpenter	
	34.	5,559,970	1996-09-24	Sharma	
	35.	5,572,691	1996-11-05	Koudmani	
	36.	5,581,498	1996-12-03	Ludwig et al.	
	37.	5,590,071	1996-12-31	Kolor et al.	
	38.	5,602,999	1997-02-11	Hyatt; Gilbert P.	
	39.	5,617,559	1997-04-01	Le et al.	
Change(s) applied to document, /S.B./ 4/28/2021	40.	5,630,096	1997-05-13	Zuravleff	
	41.	5,638,534	1997-06-10	~~Samsung Electronics Co Ltd~~	Mote, Jr.
	42.	5,649,159	1997-07-15	Le et al.	
	43.	5,655,153	1997-08-05	~~EMC CORP~~ Sandorfi	
	44.	5,699,542	1997-12-16	Mehta et al.	
	45.	5,702,984	1997-12-30	Bertin et al.	
	46.	5,703,826	1997-12-30	Hush et al.	
	47.	5,717,851	1998-02-10	Yishay et al.	
	48.	5,724,604	1998-03-03	Moyer	
	49.	5,729,716	1998-05-17	Lee et al.	
	50.	5,745,914	1998-04-28	Connolly et al.	
	51.	5,764,590	1998-06-09	~~Mitsubishi Electric Corp~~	Iwamoto et al.
	52.	5,784,705	1998-07-21	Leung, Wingyu	
	53.	5,802,395	1998-09-01	Connolly et al.	
	54.	5,802,541	1998-09-01	Reed	
	55.	5,805,520	1998-09-08	Anglada et al.	
	56.	5,822,251	1998-10-13	Bruce et al.	
	57.	5,905,401	1999-05-18	Sher	
	58.	5,909,388	1999-06-01	~~Siemens Ag~~ Mueller	
	59.	5,926,827	1999-07-20	Dell et al.	
	60.	5,926,839	1999-07-20	~~IBM~~ Katayama	
	61.	5,953,215	1999-09-14	Karabatsos, Chris	
	62.	5,953,280	1999-09-14	Matsui	
	63.	5,958,025	1999-09-28	~~Nippon Electric Co~~ Sonobe	

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed January 8, 2021*	
				Application Number	***16/695,020***
				Filing Date	***November 25, 2019***
				First Named Inventor	***Jefferey C. Solomon***
				Art Unit	***2139***
				Examiner Name	***TBD***
Sheet	1	of	47	Attorney Docket Number	***129980-5023-US01***

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date YYYY-MM-DD	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Change(s) applied to document, /S.B./ 4/28/2021	1.	4,218,740	1980-08-19	~~MOTOROLA INC~~ Bennett et al.	
	2.	4,249,253	1981-02-03	Gentili et al.	
	3.	4,368,515	1983-01-11	Nielsen	
	4.	4,392,212	1983-07-05	Miyasaka et al.	
	5.	4,571,676	1986-02-18	Mantellina et al.	
	6.	4,592,011	1986-05-27	Mantellina et al.	
	7.	4,633,429	1986-12-30	Lewandowski et al.	
	8.	4,670,748	1987-06-02	Williams	
	9.	4,706,214	1987-11-10	Mitsubishi Denki ~~Kabushiki Kaisha~~	Kassai
	10.	4,739,473	1988-04-19	Ng	
	11.	4,866,603	1989-09-02	Chiba	
	12.	4,958,322	1990-09-18	Kosugi et al.	
	13.	4,961,172	1990-10-02	Shubat et al.	
	14.	4,961,204	1990-10-02	~~Hitachi Ltd~~ Tanaka et al.	
	15.	4,980,850	1990-12-25	Morgan	
	16.	5,060,188	1991-10-22	Zulian et al.	
	17.	5,247,643	1993-09-21	Shottan	
	18.	5,272,664	1993-12-21	~~Silicon Graphics Inc~~ Alexander et al.	
	19.	5,313,624	1994-05-17	Harriman	
	20.	5,345,412	1994-09-06	Shiratsuchi	
	21.	5,357,478	1994-10-18	Kikuda et al	
	22.	5,388,072	1995-02-07	~~IBM~~ Matick et al.	
	23.	5,388,240	1995-02-01	~~IBM Corporation~~ Olderdissen et al.	
	24.	5,392,252	1995-02-21	~~Visi Technology Inc~~ Rimpo et al.	
	25.	5,426,753	1995-06-20	Moon	
	26.	5,463,590	1995-10-31	Watanabe	
	27.	5,483,497	1996-01-09	Mochizuki et al.	
	28.	5,485,589	1996-01-16	~~Dell Usa Lp~~ Kocis et al.	
	29.	5,495,435	1996-02-27	Sugahara	
	30.	5,513,135	1996-04-30	Dell et al.	

Examiner Signature	/GURTEJ BANSAL/	Date Considered	03/25/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/695,020	08/17/2021	11093417	129980-5023-US01	7514

79141 7590 07/28/2021

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 41 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Netlist, Inc., Irvine, CA;
Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Trials@uspto.gov
571-272-7822

Paper 11
Date: August 1, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00454
Patent 11,093,417 B2

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and DANIEL J. GALLIGAN, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background*

Samsung Electronics Co., Ltd. ("Petitioner") filed a petition for *inter partes* review (Paper 1 ("Pet." or "Petition")) challenging claims 1–15 of U.S. Patent 11,093,417 B2 (Ex. 1001 ("'417 patent")). Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). With our authorization (Ex. 3001), Petitioner filed a Reply to Patent Owner's Preliminary Response (Paper 9), and Patent Owner filed a Sur-reply to Petitioner's Preliminary Reply (Paper 10).

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review. The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons explained below, we institute an *inter partes* review of all challenged claims on all grounds raised in the Petition.

B. *Related Matters*

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including the following: *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex.) ("the district court litigation"); and IPR2023-00455, which involves U.S. Patent No. 9,858,215 B1, to which the '417 patent claims priority through an intervening continuation application. Pet. 1–3; Paper 4 at 1–3.

C. Real Parties in Interest

Petitioner identifies itself and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 1. Patent Owner identifies itself as the real party in interest. Paper 4 at 1.

D. The '417 Patent and Illustrative Claim

The '417 patent relates to memory modules having ranks of memory. Ex. 1001, code (57). Claim 1 is independent and is reproduced below.

> 1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:
>
> a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
>
> logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having

a non-active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices [in][1] one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

[1] The word "in" was included in an amendment under 37 C.F.R. § 1.312, which the Examiner indicated was entered. Ex. 1002, 299, 313. Thus, its omission from the issued claim appears to be the result of an error by the Office.

E. Asserted Grounds of Unpatentability

Petitioner presents the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–15	103(a)	Perego,[2] JESD79-2[3]
1–15	103(a)	Perego, JESD79-2, Ellsberry[4]
1–15	103(a)	Perego, JESD79-2, Halbert[5]

II. ANALYSIS

A. Discretionary Denial

1. 35 U.S.C. § 314(a)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 314(a) because the factors identified in *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*"), weigh in favor of denying institution in view of the district court litigation. Prelim. Resp. 62–65.

A Memorandum from Director Vidal titled *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (USPTO June 21, 2022) ("Interim Procedure")[6] provides that "the PTAB will not deny institution of an IPR or PGR under *Fintiv* . . . where a petitioner stipulates not to pursue in a parallel district

---

[2] US 7,363,422 B2, issued Apr. 22, 2008 (Ex. 1071).
[3] Joint Electron Devices Engineering Council (JEDEC) DDR2 SDRAM Specification (JESD79-2), September 2003 (Ex. 1064).
[4] US 2006/0277355 A1, published Dec. 7, 2006 (Ex. 1073).
[5] US 7,024,518 B2, issued Apr. 4, 2006 (Ex. 1078).
[6] Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition." Interim Procedure 9. Petitioner has submitted such a stipulation for all claims in this proceeding, which are all of the claims of the '417 patent. Ex. 1093; Paper 8 at 1; Paper 9 at 1. Thus, we do *not* exercise discretion to deny institution under 35 U.S.C. § 314(a).

2. 35 U.S.C. § 325(d)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 325(d) because, according to Patent Owner, the same or substantially the same prior art previously was presented to the Office. Prelim. Resp. 59–62; Paper 10 at 1–4. For the reasons stated below, we decline to exercise discretion to deny on this basis.

Section 325 of Title 35 of the United States Code addresses the relationship of proceedings before the Board with other proceedings in the Office, and provides, in part, that

> [i]n determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31,[7] the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.

35 U.S.C. § 325(d).

In evaluating arguments under Section 325(d), we use a two-part framework, determining, first, "whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office." *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*,

[7] Chapter 31 (35 U.S.C. §§ 311–319) relates to *inter partes* review.

IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential). If either condition of the first part of the framework is satisfied, we then determine "whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *Id.*

When deciding whether to exercise our discretion under Section 325(d) in view of the *Advanced Bionics* framework, we weigh the following nonexclusive factors:

> (a) the similarities and material differences between the asserted references and the prior art involved during prosecution;
>
> (b) the cumulative nature of the asserted references and the prior art evaluated during prosecution;
>
> (c) the extent to which the asserted references were evaluated during prosecution, including whether a rejection rested on any reference;
>
> (d) the extent of overlap between the arguments made during prosecution and Petitioner's reliance on the asserted references or Patent Owner's contentions concerning them;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in analyzing the asserted references; and
>
> (f) the extent to which additional evidence and facts presented in the petition warrant reconsideration of the asserted references or arguments.

See Becton, Dickinson & Co. v. B. Braun Melsungen AG, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) (formatting altered); *see also Advanced Bionics*, Paper 6 at 9–11 (noting that the Board considers the *Becton Dickinson* factors in an *Advanced Bionics* analysis).

Patent Owner argues that the first part of the *Advanced Bionics* framework is met because the same art (Ellsberry and Halbert) and substantially the same art (a continuation-in-part of Perego and a similar,

later version of JESD79-2) were disclosed during prosecution. Prelim. Resp. 60–61. Petitioner does not dispute that the asserted references or similar ones were disclosed during prosecution of the '417 patent but instead argues that it "is untenable" to "conclude that the Examiner considered them" "given the sheer number of references—***nearly 900***." Paper 9 at 1. Our precedent provides that art disclosed on an IDS is deemed to have been presented previously to the Office. *Advanced Bionics*, Paper 6 at 7–8. Thus, we determine that the same or substantially the same art previously was presented to the Office.

In the second part of the *Advanced Bionics* framework, we consider "whether the petitioner has demonstrated a material error by the Office" by evaluating *Becton Dickinson* factors (c), (e), and (f). *Advanced Bionics*, Paper 6 at 10. Petitioner argues that the claims were allowed "without any substantive rejection" and that the "Examiner identified a single reference—Janzen, ***not*** the references at issue—as the 'closest prior art.'" Paper 9 at 2; *see also* Pet. 15 ("During prosecution of the 417 Patent, the Examiner never issued a rejection and simply allowed the claims."). Petitioner contends that Patent Owner "does not (and cannot) contend that the combinations at issue are cumulative to Janzen." Paper 9 at 2. Patent Owner counters that the "pertinent question is instead whether the examiner erred in finding that Janzen is closer art than the combination, a finding that Petitioner does not contest." Paper 10 at 2.

On the record before us, we determine that *Becton Dickinson* factors (c), (e), and (f) indicate a material error by the Office. As to factor (c) (the extent to which the asserted references were evaluated during prosecution, including whether a rejection rested on any reference), the Examiner did not reject the pending claims at all, let alone based on the references asserted by

Petitioner. *See* Ex. 1002, 228 (Notice of Allowability "responsive to claims as filed dated 11/25/2019," which is the filing date of the '417 patent (Ex. 1001, code (22))). Although the asserted references were presented to the Office, the record does not indicate that there was any substantial evaluation of the references. Thus, factor (c) weighs against denying institution.

We find that factors (e) (whether Petitioner has pointed out sufficiently how the Examiner erred in analyzing the asserted references) and (f) (the extent to which additional evidence and facts presented in the petition warrant reconsideration of the asserted references or arguments) also weigh against denying institution. The Examiner's Notice of Allowability states the following:

> Janzen (US 2003/0018845) appears to be the closest prior art and teaches a memory device having a number of ranks having different burst order addressing for read and write operations. However, [Janzen] does not teach the limitation, "the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices."

Ex. 1002, 229–30 (emphasis added). With the exception of the underlined word "additional," this subject matter is recited in claim 1.

To address this subject matter, Petitioner introduces detailed testimony from Dr. Wolfe explaining how Perego, Ellsberry, and Halbert teach or suggest a larger CAS latency for the memory module than for the memory devices on the module. Ex. 1003 ¶¶ 354–378; *see* Pet. 95, 118–19,

124–26. We discuss this evidence in more detail below, but as one example, Dr. Wolfe explains that a person of ordinary skill in the art would have understood that "Perego's latching of the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer because the output of the latch needs to be in synchronization with an internal clock" and that "such registering of the data signals would require the addition of a fixed time delay, such as one clock cycle, for each registered data transfer through the circuitry with respect to the actual operational CAS latency of each of the plurality of memory integrated circuits." Ex. 1003 ¶ 360 (citing Ex. 1071, 12:65–13:5, 17:61–63, Fig. 5C).[8] As discussed below in our analysis of claim 1, we are sufficiently persuaded that this evidence supports Petitioner's contention that Perego teaches registering data for an amount of time such that the CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices. This testimony explaining how a person of ordinary skill in the art would have understood the teachings of Perego was not before the Examiner, and we find that this additional evidence warrants reconsideration of the rejection under *Becton Dickinson* factor (f) and shows that the Examiner erred in not finding a teaching in the prior art of CAS latency of the memory module being greater than an actual operational CAS latency of each of the memory devices.

For these reasons, we determine that Petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims, and we do not deny institution under 35 U.S.C. § 325(d).

---

[8] We omit the underline emphasis that Dr. Wolfe and Petitioner included for the names of prior art references.

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field" and would have had knowledge of various standards for memory, such as JEDEC, and circuitry used in memories. Pet. 9–10 (citing Ex. 1003 ¶¶ 48–50). Petitioner also contends that "[a]dditional training can substitute for educational or research experience, and vice versa." Pet. 9 (citing Ex. 1003 ¶ 48).

Patent Owner does not dispute this assessment. *See* Prelim. Resp. 6 ("For purposes of this preliminary response only, Patent Owner applies the skill level proposed by Petitioner.").

To the extent necessary, and for purposes of this Decision, we accept the uncontested assessment offered by Petitioner, except that we delete the qualifier "at least" to eliminate vagueness as to the amount of experience.

The qualifier expands the range indefinitely without an upper bound, and thus precludes a meaningful indication of the level of ordinary skill in the art.

D. Claim Construction

We interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2022).

Independent claim 1 recites memory devices arranged in ranks. Petitioner argues that a "rank" is "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module." Pet. 26 (citing Ex. 1003 ¶ 126). Patent Owner does not agree with Petitioner that a rank can include a single memory device, but Patent Owner does not explain its position because it says its arguments "are independent of that dispute." Prelim. Resp. 6.

On this record, we determine that we need not construe the term "rank" to assess whether Petitioner meets the standard for institution. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

E. Alleged Obviousness over Perego and JESD79-2 (Claims 1–15)

Petitioner asserts that claims 1–15 are unpatentable as obvious over the combined teachings of Perego and JESD79-2. Pet. 5, 28–111. Patent Owner opposes. Prelim. Resp. 13–46.

1. Overview of the Prior Art

Perego pertains to memory systems and discloses a configurable width buffer device that is coupled to memory devices and allows a data path width to be varied. Ex. 1071, code (57).

JESD79-2 is a JEDEC standard for second generation double data rate ("DDR2") memory devices. Ex. 1064.

We discuss additional pertinent details of the references in our analysis below.

2. Claim 1

Claim 1 recites a memory module having various components that are configured or configurable to operate in a particular manner, which we address in more detail below. To address the subject matter of claim 1, Petitioner relies on Perego's memory module disclosures in combination with JESD79-2's disclosures of DDR2 memory operations. Pet. 28–96. Petitioner argues that a person of ordinary skill in the art would have been motivated to combine the teachings of Perego and JESD79-2 because Perego discloses that its memory modules can use DDR2 memory devices and "the JEDEC standard for DDR2 memory devices is JESD79-2." Pet. 30 (citing Ex. 1071, 3:62–4:12, 8:1–4, 10:54–67; Ex. 1064); *see also* Pet. 30–33 (further explaining rationale to combine).

Patent Owner argues that JEDEC79-2's memory organization is incompatible with Perego's "Rambus-style memory organization." Prelim. Resp. 37–39. Patent Owner argues that these are "two distinct approaches" and cites extrinsic evidence allegedly showing that Rambus memories lack a chip select network. Prelim. Resp. 37 (citing Ex. 1069, 9, 11, 12); *see also* Prelim. Resp. 39 ("Modifying Perego to fit into the JEDEC framework that has fixed ranks and fixed bandwidth would require changing the

fundamental operating principle of Perego, which is evidence of non-obviousness.").

On this record, we are sufficiently persuaded by Petitioner's argument that a person of ordinary skill in the art would have combined the teachings of Perego and JESD79-2. As Petitioner correctly points out (Pet. 30), Perego discloses using DDR2 memory devices. Ex. 1071, 10:56–59 ("Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices."). On this record, we find this teaching to use DDR2 sufficiently supports Petitioner's rationale to combine Perego with JESD79-2, which is the JEDEC DDR2 SDRAM Specification. Ex. 1064, 1 (cover page). As to Patent Owner's argument that Rambus memories lack a chip select network (Prelim. Resp. 37), the reference on which Patent Owner relies discloses that chip select information is still used in the particular Rambus devices described. *See* Ex. 1069, 11 ("[I]n the Rambus bus organization, all addresses, commands, data, and chip-select information are sent on the same bus lines."), 12 ("[T]he example system uses a total of nine (9) lines to carry all necessary information, including addresses, commands, chip-select information, and data."). Thus, on this record, Patent Owner's focus on the lack of a chip select network, which is not recited in the claims of the '417 patent, appears misplaced. We address Patent Owner's more specific arguments below in the discussion of individual claim recitations.

a) Preamble

The preamble of claim 1 recites the following:

> A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the

memory bus including address and control signal lines and data signal lines, the memory module comprising.

Petitioner argues that Perego's Figures 3B, 3C, 4A, 4B, and 4C show memory modules that communicate data with a memory controller of a computer system via a bus. Pet. 33–39. For the recited memory commands, Petitioner cites Perego's disclosure of storing and retrieving data in response to commands, and Petitioner argues that a person of ordinary skill in the art would "have understood from their own knowledge of JEDEC standards, including JESD79-2, the specific ways to issue read and write commands to Perego's DDR2 memory devices." Pet. 39–40 (citing Ex. 1071, 6:15–25, 9:50–60, Fig. 3B; Ex. 1064, 6, 24–33, 49; Ex. 1003 ¶¶ 216–218). Petitioner argues that Perego discloses address and control lines and data lines on the memory bus. Pet. 40–41 (citing Ex. 1071, 5:12–15, 5:21–24, 9:43–45, 9:58–60, Figs. 3B, 4A, 4B; Ex. 1003 ¶¶ 220–224); *see* Ex. 1071, 5:12–15 ("One of memory subsystem ports 378a-378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a-320n."), 5:21–24 ("In other embodiments, memory subsystems are connected to a memory subsystem port via a bus (i.e., a plurality of signal lines).").

Apart from its argument that Perego and JESD79-2 would not be combined, which we address above, Patent Owner does not dispute Petitioner's contentions for the preamble.

On this record, we are sufficiently persuaded by Petitioner's contentions for the preamble, and, for purposes of institution, we need not decide whether the preamble is limiting.

b) Printed Circuit Board

Claim 1 recites "a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system." Petitioner argues that Perego's disclosure of including memory modules on printed circuit boards (PCBs) with connectors (such as connectors 390a in Figure 3C) teaches this subject matter. Pet. 42–43 (citing Ex. 1071, 5:56–6:11, 7:39–41, Figs. 3B, 3C; Ex. 1003 ¶¶ 228–233). Petitioner also argues that a person of ordinary skill in the art would have understood that Perego's memory modules could be implemented in a standard dual in-line memory module (DIMM), which would use a PCB with edge connections. Pet. 43 (citing Ex. 1071, 3:25–28, 6:34–43; Ex. 1069, 2; Ex. 1062, 29, 66; Ex. 1003 ¶ 232).

Patent Owner does not dispute Petitioner's contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

c) Logic

Claim 1 recites

> logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals.

Petitioner argues that the combination of Perego and JESD79-2 teaches this subject matter. Pet. 43–51. In particular, Petitioner argues that Perego's buffer devices in Figures 5A and 5B have logic that receives input address and control signals, which in the proposed combination would

comply with JESD79-2. Pet. 43–49 (citing Ex. 1071, 9:43–53, Figs. 4A, 4B, 5A, 5B; Ex. 1064, 6, 24–33, 49 (Table 10 (Command truth table)); Ex. 1003 ¶¶ 234–243). Petitioner argues that a person of ordinary skill in the art would have understood that "Perego's buffer device 'register[s]' address and control signals similar to a JEDEC-compliant conventional registered DIMM." Pet. 49–50 (citing Ex. 1071, 6:15–30, 13:54–59, Fig. 5C; Ex. 1062, 12; Ex. 1003 ¶¶ 239–240).

Patent Owner does not dispute the contentions summarized above but does argue that Petitioner's contentions for related limitations are deficient. We address these arguments below.

On this record, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches

> logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals,

as recited in claim 1.

d) Chip Select Signals

Claim 1 recites

> the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value.

Petitioner argues that JESD79-2 discloses read and write commands that include chip select signals to identify the target rank of memory devices. Pet. 51–52 (citing Ex. 1064, 6, 24–33, 49). Petitioner argues that it "would have been obvious to a [person of ordinary skill in the art] in light of

JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module" where the signals correspond to multiple ranks of memory devices and where one of the signals is active to select the target rank and the other signals are inactive. Pet. 57–58 (citing Ex. 1062, 6; Ex. 1066, 6–7; Ex. 1003 ¶¶ 251–252); *see also* Pet. 52–54 (explaining that chip select signal (CS) is active low). Petitioner also contends that Perego is consistent with JESD79-2's disclosure of selecting particular groups of memory devices because "Perego discloses that its module includes multiple sets of memory devices (e.g., 'ranks,' . . .), each of which can be a target of a memory read or write command, and each of which acts together in response to a memory read or write command." Pet. 54–57 (citing Ex. 1071, 6:12–24, 15:37–45, Figs. 3C, 4A, 4B, 4C; Ex. 1003 ¶¶ 249–250).

Patent Owner disputes Petitioner's contentions for this subject matter. Prelim. Resp. 13–17. Patent Owner's arguments largely fail to address the combination of teachings that Petitioner sets forth. For example, Patent Owner characterizes the Petition as arguing that, "because JEDEC-compliant DRAM devices would receive chip-select signals and DDR2 SDRAMs are compatible with Perego's invention, Perego discloses a set of input address and control signals that include 'a plurality of input chip select signals' to be received by a logic device on a DRAM module." Prelim. Resp. 13–14 (citing Pet. 51–54). Petitioner, however, does not argue that Perego discloses chip select signals. Rather, Petitioner cites JESD79-2 for its disclosure of chip select signals. *See* Pet. 51–52 (citing Ex. 1064, 6, 24–33, 49). For the reasons discussed above in § II.E.2, we disagree with Patent Owner's arguments that a person of ordinary skill in the art would not have combined the teachings of Perego and JESD79-2. *See* Prelim. Resp. 13–17.

Patent Owner also argues that

> Petitioner does not provide any competent analysis as to why Perego necessarily or even obviously employs JESD79-2 for its DDR2 SDRAM devices, nor why if it employs JESD79-2, it would then go beyond this specification and also include a chip-select bus on the memory module for providing input chip-select signals to Perego's buffer device.

Prelim. Resp. 17. On this record, we disagree with Patent Owner's arguments. Patent Owner's use of the word "necessarily" implies that Petitioner is relying on inherency, which is not the case. Rather, Petitioner argues that a person of ordinary skill in the art "would have been motivated to combine the teachings of JESD79-2 with the memory module described in Perego" because Perego discloses the use of DDR2 memories and "the JEDEC standard for DDR2 memory devices is JESD79-2." Pet. 30. As discussed above in § II.E.2, we find this reasoning sufficiently persuasive on this record.

As to Patent Owner's suggestion that "providing input chip-select signals to Perego's buffer device" would "go beyond" JESD79-2 (Prelim. Resp. 17), we are sufficiently persuaded by Petitioner's contentions that this would have been obvious based on JESD79-2 and the knowledge of other JEDEC standards. In particular, Petitioner argues that it "would have been obvious to a [person of ordinary skill in the art] in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module," citing in support JEDEC DIMM standards that show pins for receiving chip select signals at the memory module. Pet. 57–58 (citing Ex. 1003 ¶¶ 251–252, Ex. 1064, 6; Ex. 1062, 6; Ex. 1066, 6–7). Thus, Patent Owner's argument that JESD79-2 "describes the input/output to SDRAM devices, and not the

input/output to a logic device coupled between a memory controller and memory devices" (Prelim. Resp. 14 (citing Ex. 1064)) does not fully address Petitioner's contentions for this subject matter.

Patent Owner also argues that "Perego specifically contrasts the relied-on configuration with 'conventional DIMM module' designs that Petitioner suggests are JEDEC compliant." Prelim. Resp. 18 (citing Ex. 1071, 6:27–33). Although Perego draws a distinction based on the lack of buffered data lines in a conventional DIMM (Ex. 1071, 6:27–33), we do not view Perego as discounting all DIMM teachings. Indeed, as Petitioner points out (Pet. 31), Perego's goal is to preserve "[b]ackward compatibility with existing generations of memory devices," of which DIMM was one at that time. Ex. 1071, 6:37–39; *see also* Ex. 1071, 2:4–6 ("U.S. Pat. No. 5,513,135 discloses a contemporary dual inline memory module (DIMM) having one or more discrete buffer devices.").

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

e) Registered Chip Select Signal Having an Active Value

Claim 1 recites

> the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value.

Similar to its argument for the previous limitation, Petitioner argues that JESD79-2 discloses read and write commands that include a chip select signal to identify the target rank of memory devices using an active low signal with non-active ranks receiving a high signal. Pet. 58–59 (citing Ex. 1064, 6, 24–33, 49; Ex. 1003 ¶¶ 255–263). Petitioner argues that Perego is consistent with this because it "teaches that only the targeted rank of memory devices would participate in the read or write operation, while the other memory devices would 'remain in a ready or standby state until called upon to perform memory access operations.'" Pet. 59–60 (quoting Ex. 1071, 21:16–20; citing Ex. 1071, 15:40–45; Ex. 1003 ¶¶ 257–260). Petitioner argues that a person of ordinary skill in the art "would have known that under the JEDEC standards it was standard for a memory module to use registered chip-select signals to target one rank of memory devices for a read or write operation." Pet. 60 (citing Ex. 1064, 6; Ex. 1062, 12–13; Ex. 1066, 10, 12–13, Ex. 1069, 2–3; Ex. 1003 ¶ 259). Petitioner argues that Perego teaches "rank multiplication" by targeting memories on particular subsets of channels and that Perego's logic, in the combination with JESD79-2, would use the received chip select signals to select the particular targeted memories. Pet. 60–61 (citing Ex. 1003 ¶¶ 241, 261); *see also* Pet. 50–51 (discussing "rank multiplication" in Perego).

Patent Owner disputes Petitioner's contentions that it would have been obvious to send one active chip select signal with the remaining chip select signals non-active. Prelim. Resp. 26–33. In particular, Patent Owner argues that, even if Perego uses JEDEC-compliant DRAMs, the registered chip select signals sent to those devices can all be set to low (i.e., active) because other commands, such as a No Operation (NOP) command, can be used to deselect a non-targeted device. Prelim. Resp. 26–27 (citing

Ex. 1064, 48–49). Patent Owner argues that Ellsberry and Halbert suggest sending all active signals as well. Prelim. Resp. 28–29.

Patent Owner's arguments at most show that there are other suitable options for selecting particular memory devices for operations, but Petitioner's asserted combination need not present the best of those options. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) ("Our caselaw is clear. It's not necessary to show that a combination is 'the *best* option, only that it be a *suitable* option.'" quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014)). Indeed, in Patent Owner's proposed scenario in which "a non-targeted device can be sent a NOP command with a signal value of 'L' for !CS to indicate no-operation or *non-selection*" (Prelim. Resp. 27 (emphasis added)), there is still signaling that selects or deselects certain memory devices, regardless of the labels applied to such signaling.

Patent Owner also argues that Perego teaches sending commands only to targeted devices such that Perego has no need for chip select signals. Prelim. Resp. 31–33 (citing Ex. 1071, 6:12–24, 9:64–10:4, 20:41–46, 21:16–20). On this record, we are sufficiently persuaded by Petitioner's contentions that it would have been obvious to use the recited registered chip select signals based on JESD79-2's disclosure of chip select signals in DDR2 devices and Perego's disclosure of the use of DDR2s. *See* Pet. 30–33 (discussing reasons to combine), 58–61 (discussing complementary disclosures of selecting targeted memories). Patent Owner's argument that "Petitioner has not provided any competent evidence that Perego either discloses or suggests a plurality of registered chip selects signals" having different values as recited in claim 1 (Prelim. Resp. 33) ignores the asserted combination.

Patent Owner also argues that Perego's disclosures in column 15 at lines 37–45 and column 6 at lines 12–24 do not disclose chip select signals as allegedly asserted by Petitioner. Prelim. Resp. 22–25 (citing Pet. 55). Petitioner, however, does not assert that these passages disclose chip select signals. Rather, Petitioner cites these passages in support of its assertion that Perego discloses that one or more devices can be selected for an operation. *See* Pet. 54–55. Patent Owner appears to agree with this assertion when it states that in Perego "command signals are only sent to targeted memory devices." Prelim. Resp. 31 (citing Ex. 1071, 6:12–14).

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

f) Data Buffer Control Signals

Claim 1 recites "wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command." Petitioner argues that a person of ordinary skill in the art

> would have understood that Perego's buffer device includes logic that outputs data buffer control signals to transceivers (e.g., 575, included in interface 520a, 520b, 510, and 590), multiplexing/demultiplexing circuits 597, and to input/output latches 597f-m, to selectively activate these circuit elements of the "buffer" according to the targeted rank and direction of the read and write operation.

Pet. 63 (citing Ex. 1071, 14:62–15:6, 15:34–37, 17:41–44, 17:61–62, Figs. 5A, 5B; Ex. 1003 ¶¶ 270–271).

Patent Owner does not dispute Petitioner's contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

g) Ranks

Claim 1 recites "memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks."

Petitioner argues that Perego teaches memory circuits arranged in ranks by disclosing groups of memory devices that are accessed together in a memory operation. Pet. 64–73 (citing Ex. 1071, 2:4–6, 3:62–4:3, 4:19–22, 6:12–24, 8:1–4, 10:56–58, 14:10–40, 15:37–45, 17:22–28, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 274–296). For example, Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." Ex. 1071, 15:37–45, *quoted in* Pet. 67.

Petitioner provides the version of Perego's Figure 3C below.

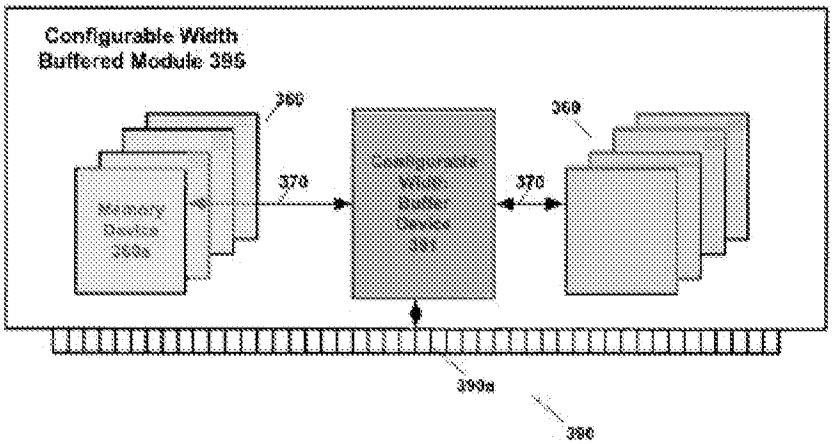

Fig. 3C

Pet. 64, 70. Perego's Figure 3C above is a block diagram of configurable width buffered module 395 having configurable width buffer device 391 (shaded red) connected on each side via channels 370 to multiple memory devices 360 (shaded green on the left and blue on the right). Ex. 1071, 2:43–45, 7:30–34; Pet. 64, 70. Noting Perego's disclosure that "one or more of channels 370" can be used in an operation (Ex. 1071, 6:12–24), Petitioner

argues that, "when Perego's buffer device has two channels, and each channel is connected to one rank, Perego's module includes two ranks of memory devices (green and blue . . .)." Pet. 69–70 (citing Ex. 1003 ¶ 283).

Petitioner also points to Perego's disclosure of a configurable width buffer having interfaces that may be programmed to have a 64-bit width by connecting to multiple devices having a total width of 64 bits. Pet. 67 (citing Ex. 1071, 14:10–15, Figs. 5A, 5B). Petitioner argues that "Perego teaches that the data width accessed in a memory transaction (W_A), and the data width of the buffer interfacing with the memory controller (W_{DP}), can both be the same (e.g., both 64 bits), such that the ratio $W_A/W_{DP} = 1{:}1$." Pet. 69 (citing Ex. 1071, 14:16–40, 17:22–28, Fig. 5C; Ex. 1003 ¶ 281). According to Petitioner, a person of ordinary skill in the art "would understand that W_A refers to the bit-width of each '*rank*' of memory devices (e.g., 64 bits can be read or written at a time) when only '***one***' of the 'one or more channels 370' . . . is used for a read or write operation." Pet. 69 (citing Ex. 1071, 6:12–24, 14:23–27, Fig. 3C; Ex. 1003 ¶¶ 282–283).

Petitioner also argues that "it would have been obvious to a [person of ordinary skill in the art] to arrange Perego's DDR memory devices into '*ranks*,' and a [person of ordinary skill in the art] would have been motivated to do so, in light of the JEDEC standards." Pet. 72 (citing Ex. 1064, 6; Ex. 1062, 13, 26–28; Ex. 1003 ¶¶ 287–289). Petitioner relies on JESD79-2's disclosure of chip select signals for ranks. Pet. 72 (citing Ex. 1064, 6; Ex. 1003 ¶¶ 287–289; Ex. 1062, 13).

Patent Owner argues that Perego does not teach "ranks" of memory devices. Prelim. Resp. 33–39. According to Patent Owner, "Petitioner has not provided any competent evidence that the devices connected to a single channel or interface 'act together' in response to a single read/write

command." Prelim. Resp. 34; *see also* Prelim. Resp. 38 ("***Perego's memory systems operate on an individual device basis***, and do not 'act together' as required by the concept of 'rank.'"). On this record, we disagree with Patent Owner.

Perego discloses that each of the interfaces in configurable width buffer device 391 of Figure 5B, on which Petitioner relies (Pet. 67–69), may connect to multiple devices, resulting in a width of 64 bits. Ex. 1071, 14:12–15; *see* Pet. 67 (discussing this disclosure). In particular, Perego discloses that "interfaces 520a and 520b may be programmed to connect to 16'x4' width memory devices, 8'x8' width memory devices or 4'x16' width memory devices." Ex. 1071, 14:12–15; *see* Pet. 67 (discussing this disclosure). Perego explains that the "maximum memory device access width" is "the largest number of bits that can be accessed in a *single memory device transfer operation* to or from configurable width buffer device 391." Ex. 1071, 14:23–27 (emphasis added). Perego also discloses that a memory operation may occur on one of channels 370. Ex. 1071, 6:12–24; *see* Pet. 69 (discussing this disclosure). On this record, in view of Perego's disclosures, we are sufficiently persuaded that, when there are multiple memory devices that account for the memory device access width (e.g., 64 bits), then those devices "act together" as in Petitioner's proposed construction. *See* Pet. 26. Furthermore, Perego discloses a serialization ratio of 1:1, meaning that the memory device access width (W_A) and the configured buffer device interface width (W_{DP}) are the same. Ex. 1071, 14:32–40, 17:22–28. In such a configuration, each rank would match the full bit-width of the memory module as in Petitioner's proposed construction. *See* Pet. 26.

Patent Owner also argues that Petitioner's contentions fail because Petitioner's "definition for a rank requires the use of chip-select signals" but

Perego "never mentions 'chip-select' signals, lines or the []like." Prelim. Resp. 36–37. Petitioner, however, relies on JESD79-2 for its disclosure of chip select signals (*see* Pet. 72), and, as noted above in § II.E.2, we are sufficiently persuaded by Petitioner's argument that a person of ordinary skill in the art would have combined the teachings of Perego and JESD79-2 given Perego's express disclosure of using DDR2, for which the industry specification is JESD79-2.

In addition to its argument that Perego discloses one rank per channel, Petitioner also argues that the memory devices connected to two channels may be considered one rank when the devices on the channels act together. Pet. 70–72 (citing Ex. 1071, 21:16–20, Figs. 4B, 4C). For example, Perego discloses, with reference to Figure 4B, that "[a]ny number of channels 415a-415d, for example, two channels 415c and 415d *may transfer information simultaneously* and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." Ex. 1071, 21:16–20 (emphasis added).

Patent Owner argues that "Petitioner does not explain why channels 415c/d together read or write ***full bit-width of the memory module*** under its own theory, given that if each channel width equals the width of the full module, two channels would have a data width twice that of the memory module." Prelim. Resp. 40–41. Petitioner's contention about using only one channel is in the context of a buffer device with two channels. *See* Pet. 69–70. We understand Petitioner's contention to be that, when there are more than two channels and memory devices on two channels act together by "transfer[ring] information simultaneously" (Ex. 1071, 21:16–20), then the data accessed in a transaction would equal the bit width of the rank (devices on the two acting channels). *See* Pet. 70–72.

Patent Owner also argues that, "although much of the Petition's theory relies on the module width being 64 bits, the data width in Perego's Figure 4B is 16 bits." Prelim. Resp. 41. Even assuming Patent Owner is correct about Figure 4B, Perego expressly discloses a 64-bit wide embodiment, as discussed above. Ex. 1071, 14:12–15; Pet. 67.

Patent Owner also argues that "Perego's modules do not have a fixed width," which Patent Owner suggests runs counter to JEDEC compliant memories. Prelim. Resp. 34–35 (citing Ex. 2003, 43:12–20); *see also* Prelim. Resp. 36 ("Nothing in the '417 patent or any JEDEC documents suggests, however, a rank of memory devices refers to a group of memory devices that is dynamically reconstituted to account for the changing memory bit width."). Patent Owner, however, does not set forth a construction of "rank" that excludes such dynamic reconfigurability. On this record, it is not clear how a device that can have many configurations, one of which satisfies the limitations of a claim, would not render obvious the subject matter of that claim merely because it is capable of additional configurations.

Patent Owner also argues that Perego's disclosure in column 15 at lines 37–45 does not teach arranging memory in ranks. Prelim. Resp. 22–23 (citing Pet. 55). For the reasons discussed above in this section, we are sufficiently persuaded that Perego teaches ranks of memory devices by its disclosures of memories that act together to read or write, which are consistent with "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." Ex. 1071, 15:37–45.

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

h) Chip Select Signals Received by Memory Devices

Claim 1 recites "wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices [in] one respective N-bit wide rank of the plurality of N-bit-wide ranks."

Petitioner argues that chip select signals would have been received by memory devices consistent with JEDEC standards. Pet. 73–74 (citing Ex. 1064, 6; Ex. 1069, 2–3; Ex. 1003 ¶¶ 297–301); *see* Ex. 1064, 6 ("Package Pinout" table showing input for Chip Select).

Patent Owner cites the following disclosure from Perego: "According to embodiments of the present invention, subsets of available memory devices on configurable width buffered module 395 are activated or powered-on during various modes of operation. Thus, configurable width buffered module 395 is able to achieve power savings by only powering particular memory devices." Ex. 1071, 20:41–46, *quoted in* Prelim. Resp. 32. Patent Owner argues that, "[i]f the non-targeted ones are not even powered on, no registered signals could be received by them." Prelim. Resp. 32. We agree with Patent Owner that, if a device does not have power, it would not operate to receive signals, but Perego does not state that every embodiment operates like this. For its part, Petitioner relies on Perego's disclosure of devices being in a "ready or standby state" to support its contention that it would have been obvious to send a non-active chip select signal to those devices. *See* Pet. 59–60 (quoting Ex. 1071, 21:16–20; citing Ex. 1071, 15:40–45). On this record, we do not understand a "ready or standby state" to be a state in which no power is supplied to the memory device. Patent Owner argues that in such a state, "no commands are sent to

the non-targeted memory devices" (Prelim. Resp. 32), but Petitioner's combination is based on chip select signals as disclosed in JESD79-2 in combination with Perego's teachings of targeting only select memories.

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

i) Receive or Output Data in Response to Memory Commands

Claim 1 recites

> wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command.

Petitioner argues that Perego teaches this subject matter because it discloses reading from or writing to a target subset of devices (rank) while other devices remain in a standby state such that they are not selected as the target devices. Pet. 74–79 (citing Ex. 1071, 6:21–22, 11:56–61, 15:31–45, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 302–323). For example, Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more independent banks)" and "rout[ing] data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer)." Ex. 1071, 15:42–45, 11:56–61. Perego also discloses that "two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." Ex. 1071, 21:16–20.

Apart from its arguments about "ranks," discussed above in § II.E.2.g, Patent Owner does not dispute Petitioner's contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner's contentions and evidence that are summarized above, and we need not address Petitioner's additional arguments based on alternative claim constructions. *See* Pet. 81–84.

j) Circuitry

Claim 1 recites

> circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;
>
> wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

Petitioner argues that Perego discloses circuitry in the buffer devices of Figures 5A and 5B that is coupled between the data signal lines in the memory bus and corresponding data pins of memory devices in each of the ranks. Pet. 85–88 (citing Ex. 1071, 4:38–42, 6:12–15, 7:30–34, 10:59–67, 11:1–7, 13:6–10, 13:18–24, 14:65–15:2, 17:61–63, 18:65–19:3, Figs. 5A, 5B, 5C; Ex. 1003 ¶¶ 324–333). Petitioner argues that Perego's data bursts are routed through the buffer device between the targeted rank of memory and the memory controller and that a person of ordinary skill in the art would have understood that buffer control signals are used "to activate only the channel transferring the data burst between the memory controller and the targeted rank" and "to selectively activate those circuit elements of the buffer according to the targeted rank and direction of the read and write

operations." Pet. 90–91 (citing Ex. 1071, 6:15–25, 11:56–61, 12:9–12, 13:54–59, 14:62–15:6, 15:34–40, 17:41–44, 17:61–62, 21:16–20, Figs. 5A, 5B; Ex. 1003 ¶¶ 338–342).

As to the "CAS latency" recitations, Petitioner argues that the data are transferred according to an overall CAS latency of the memory module, citing Perego's disclosure of "access latency values" and JESD79-2's disclosure of CAS latency values. Pet. 92–94 (citing Ex. 1071, 12:20–34, Fig. 5B; Ex. 1064, 12, 14, 26, 28, Fig. 26; Ex. 1062, 68 n.1; Ex. 1003 ¶¶ 344–353). Petitioner argues that the data transfers in Perego are registered using latches 597f–m in Figure 5C. Pet. 95–96 (citing Ex. 1071, 12:65–13:5, 17:61–63, 18:65–19:3, Figs. 5B–5C; Ex. 1003 ¶¶ 359–362). Petitioner also argues that, "[u]nder the JEDEC standards, 'an additional clock cycle' is added to the 'CAS latency' of the memory devices to leave enough time for the register on the memory module to perform its functions." Pet. 95 (citing Ex. 1062, 68 n.1; Ex. 1064, 12, 14; Ex. 1003 ¶¶ 359–362). Petitioner argues that it would have been obvious to a person of ordinary skill in the art to add an additional clock cycle in Perego "so that the memory module complies with the timing of the JEDEC standards, and so the '*circuitry*' has enough time to perform its functions (including '*register[ing]*' the data signals for interfaces 520a/b with latches 597f-m . . .) using 'internal' clock circuit 570a-b." Pet. 95 (brackets by Petitioner; citing Ex. 1071, 12:65–13:5, 17:61–63, 18:65–19:3, Figs. 5B–5C; Ex. 1003 ¶¶ 359–362).

Patent Owner disputes Petitioner's contentions for the CAS latency recitations. Prelim. Resp. 42–45. As an initial matter, for the reasons explained above in § II.E.2, we disagree with Patent Owner's argument that

a person of ordinary skill in the art would not have combined the teachings of Perego and JESD79-2. *See* Prelim. Resp. 42.

Patent Owner argues that "Perego does not state that the 'access latency values' relate to the 'overall CAS latency of the memory module,' as opposed to a latency value of the memory device itself." Prelim. Resp. 43. The relied-upon portion of Perego discloses that "serial interface 574 may be employed to couple signals utilized in initialization of *module or memory device* identification values, test function, set/reset, access latency values." Ex. 1071, 12:20–24 (emphasis added). Thus, this disclosure suggests that the access latency values may pertain to the module and memory devices on the module. *See* Ex. 1003 ¶ 346 ("Perego discloses a serial interface 574 and operation circuit 572 including a ROM . . . that, during initialization of the module, provide identification information about the module, including 'access latency values,' that are used by the controller 'to properly configure the memory devices upon boot of the system.'" (citing Ex. 1071, 12:20–34)). Based on this evidence, we are sufficiently persuaded that Perego teaches access latency values for the memory module.

Patent Owner also argues that "Petitioner has also not provided competent evidence" to show that "the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices," as recited in claim 1. Prelim. Resp. 44. We disagree. Petitioner presents detailed testimony from Dr. Wolfe explaining how Perego's registered data transfers would have introduced delay. In particular, Dr. Wolfe, citing Perego's disclosures of data latches and an internal clock to generate synchronizing clock signals (Ex. 1071, 12:65–13:5, 17:61–63, Fig. C), provides the following testimony:

> A Skilled Artisan would have understood from these disclosures that Perego's latching of the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer because the output of the latch needs to be in synchronization with an internal clock. A Skilled Artisan would have understood that such registering of the data signals would require the addition of a fixed time delay, such as one clock cycle, for each registered data transfer through the circuitry with respect to the actual operational CAS latency of each of the plurality of memory integrated circuits.

Ex. 1003 ¶ 360. Dr. Wolfe further explains how Perego's "latching delays in the buffer device of Perego increase the overall CAS latency of the memory module compared to the CAS latency of the memory devices." Ex. 1003 ¶ 362 (citing Ex. 1071, 12:65–13:5, 18:65–19:3, Figs. 5B, 5C). On this record, we find Petitioner's evidence sufficiently persuasive to show that Perego teaches that "data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices," as recited in claim 1.

We are sufficiently persuaded by Petitioner's contentions for the remainder of the "circuitry" limitation, which we summarize above and which Patent Owner does not dispute at this stage. Having determined that Petitioner presents sufficiently persuasive evidence for this subject matter, we address Patent Owner's remaining arguments regarding this subject matter.

Patent Owner argues that "Petitioner ignores that Perego's buffer device includes caches that speed up data access." Prelim. Resp. 44 (citing Ex. 1071, 12:4–9). Perego, however, indicates that such a cache is optional ("may be incorporated"). Ex. 1071, 12:4–5. Even if a cache were

incorporated, its purpose is to store the "most frequently referenced data" so that they do not have to be retrieved from memory devices, which can speed up the memory module because the cache has "lower access latency characteristics than those of the memory devices." Ex. 1071, 12:5–9. This disclosure does not speak to the latched data that are otherwise retrieved from the memory devices when such data are not present in the cache.

Patent Owner also argues that Petitioner's reliance on Additive Latency (AL) in JESD79-2 falls short because "the actual operational CAS latency of a memory device would include the AL as well as specified" CAS latency. Prelim. Resp. 45 (citing Ex. 1064, 24; Ex. 1075, 15:52–57). Thus, according to Patent Owner, the CAS latency of the memory module would equal the actual operational CAS latency of the memory device, rather than being greater than the actual operational CAS latency, as recited in claim 1. Prelim. Resp. 45. We encourage the parties to address this argument further during trial because, to the extent the JESD79-2's disclosure of AL is specific to the memory devices themselves, it would appear that this AL would impact the actual operational CAS latency of the memory device. In any case, Petitioner presents evidence that a person of ordinary skill in the art would have taken into account the latency of the entire module, including latency of the memory devices combined with latency of the buffer device. Pet. 94 (citing Ex. 1003 ¶¶ 350–351; Ex. 1062, 68 n.1). This evidence sufficiently supports Petitioner's contentions.

Patent Owner also argues that Petitioner's reliance on the DDR RDIMM specification's disclosure of adding an extra clock cycle on the memory module is misplaced because (1) "Perego expressly distinguishes its data buffer to that on a traditional RDIMM" and (2) "no similar language is found in JEDEC's DDR2 RDIMM specification." Prelim. Resp. 43 (citing

Ex. 1071, 6:27–33; Ex. 1066, 94–96; Ex. 1062, 68). As to Patent Owner's first argument, we disagree for the reasons given above in § II.E.2.d based on Perego's disclosure of wanting to maintain backward compatibility. Ex. 1071, 2:4–6, 6:27–33, 6:37–39. As to Patent Owner's second argument, some additional development of the record would be helpful during trial.

We further note that claim 1's recitation that "data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" appears to pertain to the recited "circuitry," which is "*configurable* to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module" (emphasis added). The claim, therefore, appears to require a device that is configur*able* to perform data transfers in a certain way, rather than a device that is necessarily configur*ed* to do so. Based on the evidence presented, it appears that Perego's device has such configurability. In particular, Perego discloses the following:

> According to an embodiment of the present invention, clock circuit 570a–b includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock (not shown). Clock alignment circuit may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronizing clock signals having a predetermined temporal relationship.

Ex. 1071, 12:65–13:5. Dr. Wolfe's testimony indicates that this allows Perego to "add[] a predetermined amount of time delay for each data

transfer." Ex. 1003 ¶ 360. Thus, it appears on this record that Perego discloses the configurability recited in claim 1.

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for the circuitry limitation.

k) Determination for Claim 1

For the reasons discussed above and based on Petitioner's contentions and evidence, summarized above, we are persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claim 1 is unpatentable as obvious over the combined teachings of Perego and JESD79-2. We note that Petitioner presents a short discussion of alleged secondary considerations of obviousness. Pet. 126–27. At this stage, Patent Owner does not present evidence of secondary considerations as to any of the challenged claims. Because we are sufficiently persuaded by Petitioner's showing, we need not rely on Petitioner's assertions of secondary considerations.

3. Claims 2–15

Petitioner also asserts that dependent claims 2–15 are unpatentable as obvious over the combined teachings of Perego and JESD79-2. Pet. 97–111. Patent Owner relies on the arguments addressed above in § II.E.2 and does not set forth additional arguments for claims 2–15 at this stage of the proceeding. *See* Prelim. Resp. 13–46. We have reviewed Petitioner's contentions, and we are sufficiently persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claims 2–15 are unpatentable as obvious over the combined teachings of Perego and JESD79-2.

F. Additional Grounds

As noted above, Petitioner asserts two additional grounds, each adding either Ellsberry or Halbert to the combination of Perego and JESD79-2 discussed above. Pet. 5, 111–26. Patent Owner opposes. Prelim. Resp. 45–59. Having determined that the Petition meets the threshold for institution (reasonable likelihood of prevailing as to at least one of the challenged claims) based on the Perego and JESD79-2 obviousness ground, the remainder of this Decision focuses on the parties' disputes to provide guidance to the parties for the trial.

1. Prior Art Status of Ellsberry

In an *inter partes* review, a petitioner "may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications." 35 U.S.C. § 311(b). Patent Owner argues that "patent applications are 'printed publication' prior art only as of the date they became published and available to the public." Prelim. Resp. 48. Patent Owner argues, therefore, that Ellsberry is not a prior art printed publication under 35 U.S.C. § 311(b) because it was published in December 2006, which is after the effective filing date of July 1, 2005, that Petitioner asserts applies to the '417 patent. Prelim. Resp. 46; *see* Pet. 5–6 (asserting that the claims of the '417 patent are not entitled to the benefit of a filing date before July 1, 2005).

We disagree with Patent Owner's statutory interpretation. Ellsberry is a printed publication, having been published in December 2006, as Patent Owner acknowledges. *See* Ex. 1073, code (43) (publication date of Dec. 7, 2006); *see also* Prelim. Resp. 47 (acknowledging publication date). On this record, we are persuaded by Petitioner's contentions that Ellsberry is prior

art under 35 U.S.C. § 102(e), having been filed "by another . . . in the United States before the invention by the applicant for patent." *See* Pet. 5–8 (asserting a priority date of no earlier than July 1, 2005, for the '417 patent); *see also* Ex. 1073, code (22) (filing date of June 1, 2005). Thus, Petitioner asserts a permissible ground of unpatentability under 35 U.S.C. § 311(b) by arguing that claims 1–15 are unpatentable under 35 U.S.C. § 103(a) on the basis of Ellsberry, which is a prior art printed publication, in combination with other prior art.

2. Combination of Perego, JESD79-2, and Ellsberry

Patent Owner also argues that "Ellsberry does not cure the deficiency of Perego," disputing various assertions of Petitioner as to Ellsberry's disclosure. Prelim. Resp. 48–54 (emphasis omitted). For the reasons discussed in § II.E.2, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches the subject matter of claim 1, and, therefore, on this record we do not agree with Patent Owner that there are deficiencies in the asserted combination.

With respect to Petitioner's reasoning to combine based on Ellsberry's disclosure of JEDEC compliance and DDR2 memories (Pet. 113–114), Patent Owner argues that "Petitioner does not explain why a [person of ordinary skill in the art] would modify Perego to make it comply with JEDEC." Prelim. Resp. 54. For the reasons explained above in § II.E.2, we disagree with Patent Owner.

3. Combination of Perego, JESD79-2, and Halbert

Patent Owner argues that "Halbert does not cure the deficiencies of Perego," disputing various assertions of Petitioner as to Halbert's disclosure. Prelim. Resp. 55–57. For the reasons discussed in § II.E.2, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches

the subject matter of claim 1, and, therefore, on this record we do not agree with Patent Owner that there are deficiencies in the asserted combination.

With respect to the CAS latency recitations of claim 1, Patent Owner argues the following:

> Petitioner has not pointed to any evidence that Halbert's data buffer is configured to transfer data in accordance with the overall CAS latency of the memory module, as opposed to the latency of the device after the device receives the read/write commands. Pet. 125–126. What the Petition at most shows is that due to the one-cycle delay between when the command is issued by the memory controller and when the device receives the command, the time interval between when the memory controller issues a read command and when data appears on memory bus is greater than the time interval between when the memory device receives the command and when data appears on memory bus. But that result does not evidence how the result is achieved: that is, the timing could simply result when the data buffer just transports data without reference to the overall CAS latency of memory module at all, but in reference to some other signals or parameters (e.g., the relevant data data strobe signals).

Prelim. Resp. 56–57 (citing Ex. 1078, 6:19–28).

As an initial matter, Patent Owner's argument does not appear to be commensurate in scope with the claim, which recites circuitry that is "configurable" to transfer data in a certain manner, not "configured" to do so. *See* § II.E.2.j above. Furthermore, it is unclear why Halbert's disclosure would not teach the CAS latency subject matter even if "some other signals or parameters" (Prelim. Resp. 57) cause the recited latency. In any event, we need not rely on Halbert at this stage because, for the reasons discussed above in § II.E.2.j, we are sufficiently persuaded by Petitioner's contentions based on Perego in combination with JESD79-2 for this subject matter.

Patent Owner also argues that Petitioner has not provided sufficient reasoning to combine Halbert with Perego and JESD79-2 and that Petitioner

"provides no detail whatsoever on how it suggests a [person of ordinary skill in the art] should incorporate Halbert's design in Perego." Prelim. Resp. 57–59. For claim 1, we understand Petitioner to be relying on "Halbert's disclosure of m-bit wide ranks . . . where 'm' can be 64 bits" to bolster its contention that having multiple ranks would have been obvious. Pet. 123–24. We also understand Petitioner to be relying on Halbert's disclosure of a memory module CAS latency that exceeds the CAS latency of a memory device on the module. Pet. 124–26. This latter teaching appears particularly relevant given the Examiner's reasons for allowance, which we discuss above in § II.A.2. *See* Ex. 1002, 229–30 (Examiner's reasons for allowance stating that the "closest prior art of record" does not teach the "circuitry" limitation, including the CAS latency recitations). On this record, we are sufficiently persuaded by Petitioner's reasoning that a person of ordinary skill in the art "would have recognized that the combination would have resulted in a predictable variation, which would improve similar devices like Perego in the same way and not yield unexpected results or challenges." *See* Pet. 122 (citing Ex. 1003 ¶ 198).

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging at least one claim of the '417 patent, and we institute *inter partes* review of all challenged claims on all grounds raised in the Petition. *See* 37 C.F.R. 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."). At this stage of the proceeding, we have not made a final

determination with respect to the patentability of any of the challenged claims or the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted as to claims 1–15 of the '417 patent on all challenges raised in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which will commence on the entry date of this decision.

IPR2023-00454
Patent 11,093,417 B2

FOR PETITIONER:

Eliot Williams
Theodore Chandler
Ferenc Pazmandi
John Gaustad
Brianna Potter
BAKER BOTTS LLP
eliot.williams@bakerbotts.com
ted.chandler@bakerbotts.com
ferenc.pazmandi@bakerbotts.com
john.gaustad@bakerbotts.com
brianna.potter@bakerbotts.com

FOR PATENT OWNER:

Hong Zhong
Jonathan Lindsay
IRELL & MANELLA LLP
hzhong@irell.com
jlindsay@irell.com

Trials@uspto.gov
571-272-7822

Paper 11
Date: August 1, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00454
Patent 11,093,417 B2

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and DANIEL J. GALLIGAN, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background*

Samsung Electronics Co., Ltd. ("Petitioner") filed a petition for *inter partes* review (Paper 1 ("Pet." or "Petition")) challenging claims 1–15 of U.S. Patent 11,093,417 B2 (Ex. 1001 ("'417 patent")). Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). With our authorization (Ex. 3001), Petitioner filed a Reply to Patent Owner's Preliminary Response (Paper 9), and Patent Owner filed a Sur-reply to Petitioner's Preliminary Reply (Paper 10).

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review. The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons explained below, we institute an *inter partes* review of all challenged claims on all grounds raised in the Petition.

B. *Related Matters*

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including the following: *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex.) ("the district court litigation"); and IPR2023-00455, which involves U.S. Patent No. 9,858,215 B1, to which the '417 patent claims priority through an intervening continuation application. Pet. 1–3; Paper 4 at 1–3.

C. Real Parties in Interest

Petitioner identifies itself and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 1. Patent Owner identifies itself as the real party in interest. Paper 4 at 1.

D. The '417 Patent and Illustrative Claim

The '417 patent relates to memory modules having ranks of memory. Ex. 1001, code (57). Claim 1 is independent and is reproduced below.

> 1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:
>
> a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
>
> logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having

a non-active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices [in][1] one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

[1] The word "in" was included in an amendment under 37 C.F.R. § 1.312, which the Examiner indicated was entered. Ex. 1002, 299, 313. Thus, its omission from the issued claim appears to be the result of an error by the Office.

E. Asserted Grounds of Unpatentability

Petitioner presents the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–15	103(a)	Perego,[2] JESD79-2[3]
1–15	103(a)	Perego, JESD79-2, Ellsberry[4]
1–15	103(a)	Perego, JESD79-2, Halbert[5]

II. ANALYSIS

A. Discretionary Denial

1. 35 U.S.C. § 314(a)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 314(a) because the factors identified in *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*"), weigh in favor of denying institution in view of the district court litigation. Prelim. Resp. 62–65.

A Memorandum from Director Vidal titled *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (USPTO June 21, 2022) ("Interim Procedure")[6] provides that "the PTAB will not deny institution of an IPR or PGR under *Fintiv* . . . where a petitioner stipulates not to pursue in a parallel district

---

[2] US 7,363,422 B2, issued Apr. 22, 2008 (Ex. 1071).
[3] Joint Electron Devices Engineering Council (JEDEC) DDR2 SDRAM Specification (JESD79-2), September 2003 (Ex. 1064).
[4] US 2006/0277355 A1, published Dec. 7, 2006 (Ex. 1073).
[5] US 7,024,518 B2, issued Apr. 4, 2006 (Ex. 1078).
[6] Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition." Interim Procedure 9. Petitioner has submitted such a stipulation for all claims in this proceeding, which are all of the claims of the '417 patent. Ex. 1093; Paper 8 at 1; Paper 9 at 1. Thus, we do *not* exercise discretion to deny institution under 35 U.S.C. § 314(a).

2. 35 U.S.C. § 325(d)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 325(d) because, according to Patent Owner, the same or substantially the same prior art previously was presented to the Office. Prelim. Resp. 59–62; Paper 10 at 1–4. For the reasons stated below, we decline to exercise discretion to deny on this basis.

Section 325 of Title 35 of the United States Code addresses the relationship of proceedings before the Board with other proceedings in the Office, and provides, in part, that

> [i]n determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31,[7] the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.

35 U.S.C. § 325(d).

In evaluating arguments under Section 325(d), we use a two-part framework, determining, first, "whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office." *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*,

[7] Chapter 31 (35 U.S.C. §§ 311–319) relates to *inter partes* review.

IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential). If either condition of the first part of the framework is satisfied, we then determine "whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *Id.*

When deciding whether to exercise our discretion under Section 325(d) in view of the *Advanced Bionics* framework, we weigh the following nonexclusive factors:

> (a) the similarities and material differences between the asserted references and the prior art involved during prosecution;
>
> (b) the cumulative nature of the asserted references and the prior art evaluated during prosecution;
>
> (c) the extent to which the asserted references were evaluated during prosecution, including whether a rejection rested on any reference;
>
> (d) the extent of overlap between the arguments made during prosecution and Petitioner's reliance on the asserted references or Patent Owner's contentions concerning them;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in analyzing the asserted references; and
>
> (f) the extent to which additional evidence and facts presented in the petition warrant reconsideration of the asserted references or arguments.

See Becton, Dickinson & Co. v. B. Braun Melsungen AG, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) (formatting altered); *see also Advanced Bionics*, Paper 6 at 9–11 (noting that the Board considers the *Becton Dickinson* factors in an *Advanced Bionics* analysis).

Patent Owner argues that the first part of the *Advanced Bionics* framework is met because the same art (Ellsberry and Halbert) and substantially the same art (a continuation-in-part of Perego and a similar,

later version of JESD79-2) were disclosed during prosecution. Prelim. Resp. 60–61. Petitioner does not dispute that the asserted references or similar ones were disclosed during prosecution of the '417 patent but instead argues that it "is untenable" to "conclude that the Examiner considered them" "given the sheer number of references—***nearly 900***." Paper 9 at 1. Our precedent provides that art disclosed on an IDS is deemed to have been presented previously to the Office. *Advanced Bionics*, Paper 6 at 7–8. Thus, we determine that the same or substantially the same art previously was presented to the Office.

In the second part of the *Advanced Bionics* framework, we consider "whether the petitioner has demonstrated a material error by the Office" by evaluating *Becton Dickinson* factors (c), (e), and (f). *Advanced Bionics*, Paper 6 at 10. Petitioner argues that the claims were allowed "without any substantive rejection" and that the "Examiner identified a single reference—Janzen, ***not*** the references at issue—as the 'closest prior art.'" Paper 9 at 2; *see also* Pet. 15 ("During prosecution of the 417 Patent, the Examiner never issued a rejection and simply allowed the claims."). Petitioner contends that Patent Owner "does not (and cannot) contend that the combinations at issue are cumulative to Janzen." Paper 9 at 2. Patent Owner counters that the "pertinent question is instead whether the examiner erred in finding that Janzen is closer art than the combination, a finding that Petitioner does not contest." Paper 10 at 2.

On the record before us, we determine that *Becton Dickinson* factors (c), (e), and (f) indicate a material error by the Office. As to factor (c) (the extent to which the asserted references were evaluated during prosecution, including whether a rejection rested on any reference), the Examiner did not reject the pending claims at all, let alone based on the references asserted by

Petitioner. *See* Ex. 1002, 228 (Notice of Allowability "responsive to claims as filed dated 11/25/2019," which is the filing date of the '417 patent (Ex. 1001, code (22))). Although the asserted references were presented to the Office, the record does not indicate that there was any substantial evaluation of the references. Thus, factor (c) weighs against denying institution.

We find that factors (e) (whether Petitioner has pointed out sufficiently how the Examiner erred in analyzing the asserted references) and (f) (the extent to which additional evidence and facts presented in the petition warrant reconsideration of the asserted references or arguments) also weigh against denying institution. The Examiner's Notice of Allowability states the following:

> Janzen (US 2003/0018845) appears to be the closest prior art and teaches a memory device having a number of ranks having different burst order addressing for read and write operations. However, [Janzen] does not teach the limitation, "the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices."

Ex. 1002, 229–30 (emphasis added). With the exception of the underlined word "additional," this subject matter is recited in claim 1.

To address this subject matter, Petitioner introduces detailed testimony from Dr. Wolfe explaining how Perego, Ellsberry, and Halbert teach or suggest a larger CAS latency for the memory module than for the memory devices on the module. Ex. 1003 ¶¶ 354–378; *see* Pet. 95, 118–19,

124–26. We discuss this evidence in more detail below, but as one example, Dr. Wolfe explains that a person of ordinary skill in the art would have understood that "Perego's latching of the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer because the output of the latch needs to be in synchronization with an internal clock" and that "such registering of the data signals would require the addition of a fixed time delay, such as one clock cycle, for each registered data transfer through the circuitry with respect to the actual operational CAS latency of each of the plurality of memory integrated circuits." Ex. 1003 ¶ 360 (citing Ex. 1071, 12:65–13:5, 17:61–63, Fig. 5C).[8] As discussed below in our analysis of claim 1, we are sufficiently persuaded that this evidence supports Petitioner's contention that Perego teaches registering data for an amount of time such that the CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices. This testimony explaining how a person of ordinary skill in the art would have understood the teachings of Perego was not before the Examiner, and we find that this additional evidence warrants reconsideration of the rejection under *Becton Dickinson* factor (f) and shows that the Examiner erred in not finding a teaching in the prior art of CAS latency of the memory module being greater than an actual operational CAS latency of each of the memory devices.

For these reasons, we determine that Petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims, and we do not deny institution under 35 U.S.C. § 325(d).

---

[8] We omit the underline emphasis that Dr. Wolfe and Petitioner included for the names of prior art references.

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field" and would have had knowledge of various standards for memory, such as JEDEC, and circuitry used in memories. Pet. 9–10 (citing Ex. 1003 ¶¶ 48–50). Petitioner also contends that "[a]dditional training can substitute for educational or research experience, and vice versa." Pet. 9 (citing Ex. 1003 ¶ 48).

Patent Owner does not dispute this assessment. *See* Prelim. Resp. 6 ("For purposes of this preliminary response only, Patent Owner applies the skill level proposed by Petitioner.").

To the extent necessary, and for purposes of this Decision, we accept the uncontested assessment offered by Petitioner, except that we delete the qualifier "at least" to eliminate vagueness as to the amount of experience.

The qualifier expands the range indefinitely without an upper bound, and thus precludes a meaningful indication of the level of ordinary skill in the art.

D. Claim Construction

We interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2022).

Independent claim 1 recites memory devices arranged in ranks. Petitioner argues that a "rank" is "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module." Pet. 26 (citing Ex. 1003 ¶ 126). Patent Owner does not agree with Petitioner that a rank can include a single memory device, but Patent Owner does not explain its position because it says its arguments "are independent of that dispute." Prelim. Resp. 6.

On this record, we determine that we need not construe the term "rank" to assess whether Petitioner meets the standard for institution. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

E. Alleged Obviousness over Perego and JESD79-2 (Claims 1–15)

Petitioner asserts that claims 1–15 are unpatentable as obvious over the combined teachings of Perego and JESD79-2. Pet. 5, 28–111. Patent Owner opposes. Prelim. Resp. 13–46.

1. Overview of the Prior Art

Perego pertains to memory systems and discloses a configurable width buffer device that is coupled to memory devices and allows a data path width to be varied. Ex. 1071, code (57).

JESD79-2 is a JEDEC standard for second generation double data rate ("DDR2") memory devices. Ex. 1064.

We discuss additional pertinent details of the references in our analysis below.

2. Claim 1

Claim 1 recites a memory module having various components that are configured or configurable to operate in a particular manner, which we address in more detail below. To address the subject matter of claim 1, Petitioner relies on Perego's memory module disclosures in combination with JESD79-2's disclosures of DDR2 memory operations. Pet. 28–96. Petitioner argues that a person of ordinary skill in the art would have been motivated to combine the teachings of Perego and JESD79-2 because Perego discloses that its memory modules can use DDR2 memory devices and "the JEDEC standard for DDR2 memory devices is JESD79-2." Pet. 30 (citing Ex. 1071, 3:62–4:12, 8:1–4, 10:54–67; Ex. 1064); *see also* Pet. 30–33 (further explaining rationale to combine).

Patent Owner argues that JEDEC79-2's memory organization is incompatible with Perego's "Rambus-style memory organization." Prelim. Resp. 37–39. Patent Owner argues that these are "two distinct approaches" and cites extrinsic evidence allegedly showing that Rambus memories lack a chip select network. Prelim. Resp. 37 (citing Ex. 1069, 9, 11, 12); *see also* Prelim. Resp. 39 ("Modifying Perego to fit into the JEDEC framework that has fixed ranks and fixed bandwidth would require changing the

fundamental operating principle of Perego, which is evidence of non-obviousness.").

On this record, we are sufficiently persuaded by Petitioner's argument that a person of ordinary skill in the art would have combined the teachings of Perego and JESD79-2. As Petitioner correctly points out (Pet. 30), Perego discloses using DDR2 memory devices. Ex. 1071, 10:56–59 ("Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices."). On this record, we find this teaching to use DDR2 sufficiently supports Petitioner's rationale to combine Perego with JESD79-2, which is the JEDEC DDR2 SDRAM Specification. Ex. 1064, 1 (cover page). As to Patent Owner's argument that Rambus memories lack a chip select network (Prelim. Resp. 37), the reference on which Patent Owner relies discloses that chip select information is still used in the particular Rambus devices described. *See* Ex. 1069, 11 ("[I]n the Rambus bus organization, all addresses, commands, data, and chip-select information are sent on the same bus lines."), 12 ("[T]he example system uses a total of nine (9) lines to carry all necessary information, including addresses, commands, chip-select information, and data."). Thus, on this record, Patent Owner's focus on the lack of a chip select network, which is not recited in the claims of the '417 patent, appears misplaced. We address Patent Owner's more specific arguments below in the discussion of individual claim recitations.

a) Preamble

The preamble of claim 1 recites the following:

> A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the

memory bus including address and control signal lines and data signal lines, the memory module comprising.

Petitioner argues that Perego's Figures 3B, 3C, 4A, 4B, and 4C show memory modules that communicate data with a memory controller of a computer system via a bus. Pet. 33–39. For the recited memory commands, Petitioner cites Perego's disclosure of storing and retrieving data in response to commands, and Petitioner argues that a person of ordinary skill in the art would "have understood from their own knowledge of JEDEC standards, including JESD79-2, the specific ways to issue read and write commands to Perego's DDR2 memory devices." Pet. 39–40 (citing Ex. 1071, 6:15–25, 9:50–60, Fig. 3B; Ex. 1064, 6, 24–33, 49; Ex. 1003 ¶¶ 216–218). Petitioner argues that Perego discloses address and control lines and data lines on the memory bus. Pet. 40–41 (citing Ex. 1071, 5:12–15, 5:21–24, 9:43–45, 9:58–60, Figs. 3B, 4A, 4B; Ex. 1003 ¶¶ 220–224); *see* Ex. 1071, 5:12–15 ("One of memory subsystem ports 378a-378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a-320n."), 5:21–24 ("In other embodiments, memory subsystems are connected to a memory subsystem port via a bus (i.e., a plurality of signal lines).").

Apart from its argument that Perego and JESD79-2 would not be combined, which we address above, Patent Owner does not dispute Petitioner's contentions for the preamble.

On this record, we are sufficiently persuaded by Petitioner's contentions for the preamble, and, for purposes of institution, we need not decide whether the preamble is limiting.

b) Printed Circuit Board

Claim 1 recites "a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system." Petitioner argues that Perego's disclosure of including memory modules on printed circuit boards (PCBs) with connectors (such as connectors 390a in Figure 3C) teaches this subject matter. Pet. 42–43 (citing Ex. 1071, 5:56–6:11, 7:39–41, Figs. 3B, 3C; Ex. 1003 ¶¶ 228–233). Petitioner also argues that a person of ordinary skill in the art would have understood that Perego's memory modules could be implemented in a standard dual in-line memory module (DIMM), which would use a PCB with edge connections. Pet. 43 (citing Ex. 1071, 3:25–28, 6:34–43; Ex. 1069, 2; Ex. 1062, 29, 66; Ex. 1003 ¶ 232).

Patent Owner does not dispute Petitioner's contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

c) Logic

Claim 1 recites

> logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals.

Petitioner argues that the combination of Perego and JESD79-2 teaches this subject matter. Pet. 43–51. In particular, Petitioner argues that Perego's buffer devices in Figures 5A and 5B have logic that receives input address and control signals, which in the proposed combination would

comply with JESD79-2. Pet. 43–49 (citing Ex. 1071, 9:43–53, Figs. 4A, 4B, 5A, 5B; Ex. 1064, 6, 24–33, 49 (Table 10 (Command truth table)); Ex. 1003 ¶¶ 234–243). Petitioner argues that a person of ordinary skill in the art would have understood that "Perego's buffer device 'register[s]' address and control signals similar to a JEDEC-compliant conventional registered DIMM." Pet. 49–50 (citing Ex. 1071, 6:15–30, 13:54–59, Fig. 5C; Ex. 1062, 12; Ex. 1003 ¶¶ 239–240).

Patent Owner does not dispute the contentions summarized above but does argue that Petitioner's contentions for related limitations are deficient. We address these arguments below.

On this record, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches

> logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals,

as recited in claim 1.

d) Chip Select Signals

Claim 1 recites

> the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value.

Petitioner argues that JESD79-2 discloses read and write commands that include chip select signals to identify the target rank of memory devices. Pet. 51–52 (citing Ex. 1064, 6, 24–33, 49). Petitioner argues that it "would have been obvious to a [person of ordinary skill in the art] in light of

JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module" where the signals correspond to multiple ranks of memory devices and where one of the signals is active to select the target rank and the other signals are inactive. Pet. 57–58 (citing Ex. 1062, 6; Ex. 1066, 6–7; Ex. 1003 ¶¶ 251–252); *see also* Pet. 52–54 (explaining that chip select signal (CS) is active low). Petitioner also contends that Perego is consistent with JESD79-2's disclosure of selecting particular groups of memory devices because "Perego discloses that its module includes multiple sets of memory devices (e.g., 'ranks,' . . .), each of which can be a target of a memory read or write command, and each of which acts together in response to a memory read or write command." Pet. 54–57 (citing Ex. 1071, 6:12–24, 15:37–45, Figs. 3C, 4A, 4B, 4C; Ex. 1003 ¶¶ 249–250).

Patent Owner disputes Petitioner's contentions for this subject matter. Prelim. Resp. 13–17. Patent Owner's arguments largely fail to address the combination of teachings that Petitioner sets forth. For example, Patent Owner characterizes the Petition as arguing that, "because JEDEC-compliant DRAM devices would receive chip-select signals and DDR2 SDRAMs are compatible with Perego's invention, Perego discloses a set of input address and control signals that include 'a plurality of input chip select signals' to be received by a logic device on a DRAM module." Prelim. Resp. 13–14 (citing Pet. 51–54). Petitioner, however, does not argue that Perego discloses chip select signals. Rather, Petitioner cites JESD79-2 for its disclosure of chip select signals. *See* Pet. 51–52 (citing Ex. 1064, 6, 24–33, 49). For the reasons discussed above in § II.E.2, we disagree with Patent Owner's arguments that a person of ordinary skill in the art would not have combined the teachings of Perego and JESD79-2. *See* Prelim. Resp. 13–17.

Patent Owner also argues that

> Petitioner does not provide any competent analysis as to why Perego necessarily or even obviously employs JESD79-2 for its DDR2 SDRAM devices, nor why if it employs JESD79-2, it would then go beyond this specification and also include a chip-select bus on the memory module for providing input chip-select signals to Perego's buffer device.

Prelim. Resp. 17. On this record, we disagree with Patent Owner's arguments. Patent Owner's use of the word "necessarily" implies that Petitioner is relying on inherency, which is not the case. Rather, Petitioner argues that a person of ordinary skill in the art "would have been motivated to combine the teachings of JESD79-2 with the memory module described in Perego" because Perego discloses the use of DDR2 memories and "the JEDEC standard for DDR2 memory devices is JESD79-2." Pet. 30. As discussed above in § II.E.2, we find this reasoning sufficiently persuasive on this record.

As to Patent Owner's suggestion that "providing input chip-select signals to Perego's buffer device" would "go beyond" JESD79-2 (Prelim. Resp. 17), we are sufficiently persuaded by Petitioner's contentions that this would have been obvious based on JESD79-2 and the knowledge of other JEDEC standards. In particular, Petitioner argues that it "would have been obvious to a [person of ordinary skill in the art] in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module," citing in support JEDEC DIMM standards that show pins for receiving chip select signals at the memory module. Pet. 57–58 (citing Ex. 1003 ¶¶ 251–252, Ex. 1064, 6; Ex. 1062, 6; Ex. 1066, 6–7). Thus, Patent Owner's argument that JESD79-2 "describes the input/output to SDRAM devices, and not the

input/output to a logic device coupled between a memory controller and memory devices" (Prelim. Resp. 14 (citing Ex. 1064)) does not fully address Petitioner's contentions for this subject matter.

Patent Owner also argues that "Perego specifically contrasts the relied-on configuration with 'conventional DIMM module' designs that Petitioner suggests are JEDEC compliant." Prelim. Resp. 18 (citing Ex. 1071, 6:27–33). Although Perego draws a distinction based on the lack of buffered data lines in a conventional DIMM (Ex. 1071, 6:27–33), we do not view Perego as discounting all DIMM teachings. Indeed, as Petitioner points out (Pet. 31), Perego's goal is to preserve "[b]ackward compatibility with existing generations of memory devices," of which DIMM was one at that time. Ex. 1071, 6:37–39; *see also* Ex. 1071, 2:4–6 ("U.S. Pat. No. 5,513,135 discloses a contemporary dual inline memory module (DIMM) having one or more discrete buffer devices.").

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

e) Registered Chip Select Signal Having an Active Value

Claim 1 recites

> the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value.

Similar to its argument for the previous limitation, Petitioner argues that JESD79-2 discloses read and write commands that include a chip select signal to identify the target rank of memory devices using an active low signal with non-active ranks receiving a high signal. Pet. 58–59 (citing Ex. 1064, 6, 24–33, 49; Ex. 1003 ¶¶ 255–263). Petitioner argues that Perego is consistent with this because it "teaches that only the targeted rank of memory devices would participate in the read or write operation, while the other memory devices would 'remain in a ready or standby state until called upon to perform memory access operations.'" Pet. 59–60 (quoting Ex. 1071, 21:16–20; citing Ex. 1071, 15:40–45; Ex. 1003 ¶¶ 257–260). Petitioner argues that a person of ordinary skill in the art "would have known that under the JEDEC standards it was standard for a memory module to use registered chip-select signals to target one rank of memory devices for a read or write operation." Pet. 60 (citing Ex. 1064, 6; Ex. 1062, 12–13; Ex. 1066, 10, 12–13, Ex. 1069, 2–3; Ex. 1003 ¶ 259). Petitioner argues that Perego teaches "rank multiplication" by targeting memories on particular subsets of channels and that Perego's logic, in the combination with JESD79-2, would use the received chip select signals to select the particular targeted memories. Pet. 60–61 (citing Ex. 1003 ¶¶ 241, 261); *see also* Pet. 50–51 (discussing "rank multiplication" in Perego).

Patent Owner disputes Petitioner's contentions that it would have been obvious to send one active chip select signal with the remaining chip select signals non-active. Prelim. Resp. 26–33. In particular, Patent Owner argues that, even if Perego uses JEDEC-compliant DRAMs, the registered chip select signals sent to those devices can all be set to low (i.e., active) because other commands, such as a No Operation (NOP) command, can be used to deselect a non-targeted device. Prelim. Resp. 26–27 (citing

Ex. 1064, 48–49). Patent Owner argues that Ellsberry and Halbert suggest sending all active signals as well. Prelim. Resp. 28–29.

Patent Owner's arguments at most show that there are other suitable options for selecting particular memory devices for operations, but Petitioner's asserted combination need not present the best of those options. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) ("Our caselaw is clear. It's not necessary to show that a combination is 'the *best* option, only that it be a *suitable* option.'" quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014)). Indeed, in Patent Owner's proposed scenario in which "a non-targeted device can be sent a NOP command with a signal value of 'L' for !CS to indicate no-operation or *non-selection*" (Prelim. Resp. 27 (emphasis added)), there is still signaling that selects or deselects certain memory devices, regardless of the labels applied to such signaling.

Patent Owner also argues that Perego teaches sending commands only to targeted devices such that Perego has no need for chip select signals. Prelim. Resp. 31–33 (citing Ex. 1071, 6:12–24, 9:64–10:4, 20:41–46, 21:16–20). On this record, we are sufficiently persuaded by Petitioner's contentions that it would have been obvious to use the recited registered chip select signals based on JESD79-2's disclosure of chip select signals in DDR2 devices and Perego's disclosure of the use of DDR2s. *See* Pet. 30–33 (discussing reasons to combine), 58–61 (discussing complementary disclosures of selecting targeted memories). Patent Owner's argument that "Petitioner has not provided any competent evidence that Perego either discloses or suggests a plurality of registered chip selects signals" having different values as recited in claim 1 (Prelim. Resp. 33) ignores the asserted combination.

Patent Owner also argues that Perego's disclosures in column 15 at lines 37–45 and column 6 at lines 12–24 do not disclose chip select signals as allegedly asserted by Petitioner. Prelim. Resp. 22–25 (citing Pet. 55). Petitioner, however, does not assert that these passages disclose chip select signals. Rather, Petitioner cites these passages in support of its assertion that Perego discloses that one or more devices can be selected for an operation. *See* Pet. 54–55. Patent Owner appears to agree with this assertion when it states that in Perego "command signals are only sent to targeted memory devices." Prelim. Resp. 31 (citing Ex. 1071, 6:12–14).

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

f) Data Buffer Control Signals

Claim 1 recites "wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command." Petitioner argues that a person of ordinary skill in the art

> would have understood that Perego's buffer device includes logic that outputs data buffer control signals to transceivers (e.g., 575, included in interface 520a, 520b, 510, and 590), multiplexing/demultiplexing circuits 597, and to input/output latches 597f-m, to selectively activate these circuit elements of the "buffer" according to the targeted rank and direction of the read and write operation.

Pet. 63 (citing Ex. 1071, 14:62–15:6, 15:34–37, 17:41–44, 17:61–62, Figs. 5A, 5B; Ex. 1003 ¶¶ 270–271).

Patent Owner does not dispute Petitioner's contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

g) Ranks

Claim 1 recites "memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks."

Petitioner argues that Perego teaches memory circuits arranged in ranks by disclosing groups of memory devices that are accessed together in a memory operation. Pet. 64–73 (citing Ex. 1071, 2:4–6, 3:62–4:3, 4:19–22, 6:12–24, 8:1–4, 10:56–58, 14:10–40, 15:37–45, 17:22–28, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 274–296). For example, Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." Ex. 1071, 15:37–45, *quoted in* Pet. 67.

Petitioner provides the version of Perego's Figure 3C below.

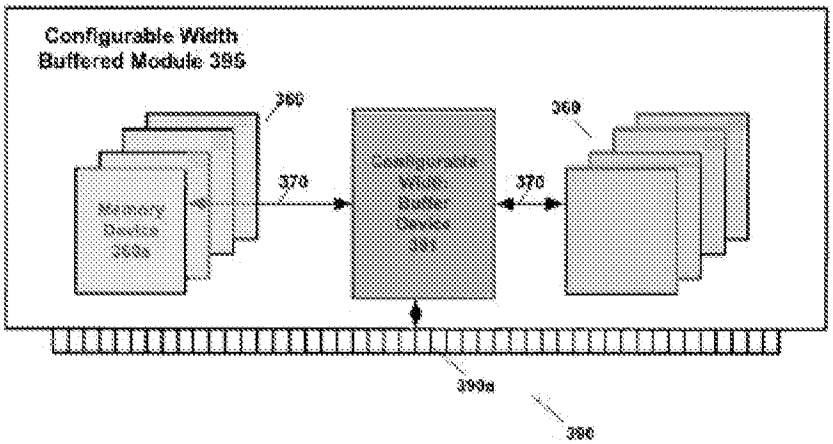

Fig. 3C

Pet. 64, 70. Perego's Figure 3C above is a block diagram of configurable width buffered module 395 having configurable width buffer device 391 (shaded red) connected on each side via channels 370 to multiple memory devices 360 (shaded green on the left and blue on the right). Ex. 1071, 2:43–45, 7:30–34; Pet. 64, 70. Noting Perego's disclosure that "one or more of channels 370" can be used in an operation (Ex. 1071, 6:12–24), Petitioner

argues that, "when Perego's buffer device has two channels, and each channel is connected to one rank, Perego's module includes two ranks of memory devices (green and blue . . .)." Pet. 69–70 (citing Ex. 1003 ¶ 283).

Petitioner also points to Perego's disclosure of a configurable width buffer having interfaces that may be programmed to have a 64-bit width by connecting to multiple devices having a total width of 64 bits. Pet. 67 (citing Ex. 1071, 14:10–15, Figs. 5A, 5B). Petitioner argues that "Perego teaches that the data width accessed in a memory transaction (W_A), and the data width of the buffer interfacing with the memory controller (W_{DP}), can both be the same (e.g., both 64 bits), such that the ratio $W_A/W_{DP} = 1{:}1$." Pet. 69 (citing Ex. 1071, 14:16–40, 17:22–28, Fig. 5C; Ex. 1003 ¶ 281). According to Petitioner, a person of ordinary skill in the art "would understand that W_A refers to the bit-width of each '*rank*' of memory devices (e.g., 64 bits can be read or written at a time) when only '***one***' of the 'one or more channels 370' . . . is used for a read or write operation." Pet. 69 (citing Ex. 1071, 6:12–24, 14:23–27, Fig. 3C; Ex. 1003 ¶¶ 282–283).

Petitioner also argues that "it would have been obvious to a [person of ordinary skill in the art] to arrange Perego's DDR memory devices into '*ranks*,' and a [person of ordinary skill in the art] would have been motivated to do so, in light of the JEDEC standards." Pet. 72 (citing Ex. 1064, 6; Ex. 1062, 13, 26–28; Ex. 1003 ¶¶ 287–289). Petitioner relies on JESD79-2's disclosure of chip select signals for ranks. Pet. 72 (citing Ex. 1064, 6; Ex. 1003 ¶¶ 287–289; Ex. 1062, 13).

Patent Owner argues that Perego does not teach "ranks" of memory devices. Prelim. Resp. 33–39. According to Patent Owner, "Petitioner has not provided any competent evidence that the devices connected to a single channel or interface 'act together' in response to a single read/write

command." Prelim. Resp. 34; *see also* Prelim. Resp. 38 ("***Perego's memory systems operate on an individual device basis***, and do not 'act together' as required by the concept of 'rank.'"). On this record, we disagree with Patent Owner.

Perego discloses that each of the interfaces in configurable width buffer device 391 of Figure 5B, on which Petitioner relies (Pet. 67–69), may connect to multiple devices, resulting in a width of 64 bits. Ex. 1071, 14:12–15; *see* Pet. 67 (discussing this disclosure). In particular, Perego discloses that "interfaces 520a and 520b may be programmed to connect to 16'x4' width memory devices, 8'x8' width memory devices or 4'x16' width memory devices." Ex. 1071, 14:12–15; *see* Pet. 67 (discussing this disclosure). Perego explains that the "maximum memory device access width" is "the largest number of bits that can be accessed in a *single memory device transfer operation* to or from configurable width buffer device 391." Ex. 1071, 14:23–27 (emphasis added). Perego also discloses that a memory operation may occur on one of channels 370. Ex. 1071, 6:12–24; *see* Pet. 69 (discussing this disclosure). On this record, in view of Perego's disclosures, we are sufficiently persuaded that, when there are multiple memory devices that account for the memory device access width (e.g., 64 bits), then those devices "act together" as in Petitioner's proposed construction. *See* Pet. 26. Furthermore, Perego discloses a serialization ratio of 1:1, meaning that the memory device access width (W_A) and the configured buffer device interface width (W_{DP}) are the same. Ex. 1071, 14:32–40, 17:22–28. In such a configuration, each rank would match the full bit-width of the memory module as in Petitioner's proposed construction. *See* Pet. 26.

Patent Owner also argues that Petitioner's contentions fail because Petitioner's "definition for a rank requires the use of chip-select signals" but

Perego "never mentions 'chip-select' signals, lines or the []like." Prelim. Resp. 36–37. Petitioner, however, relies on JESD79-2 for its disclosure of chip select signals (*see* Pet. 72), and, as noted above in § II.E.2, we are sufficiently persuaded by Petitioner's argument that a person of ordinary skill in the art would have combined the teachings of Perego and JESD79-2 given Perego's express disclosure of using DDR2, for which the industry specification is JESD79-2.

In addition to its argument that Perego discloses one rank per channel, Petitioner also argues that the memory devices connected to two channels may be considered one rank when the devices on the channels act together. Pet. 70–72 (citing Ex. 1071, 21:16–20, Figs. 4B, 4C). For example, Perego discloses, with reference to Figure 4B, that "[a]ny number of channels 415a-415d, for example, two channels 415c and 415d *may transfer information simultaneously* and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." Ex. 1071, 21:16–20 (emphasis added).

Patent Owner argues that "Petitioner does not explain why channels 415c/d together read or write ***full bit-width of the memory module*** under its own theory, given that if each channel width equals the width of the full module, two channels would have a data width twice that of the memory module." Prelim. Resp. 40–41. Petitioner's contention about using only one channel is in the context of a buffer device with two channels. *See* Pet. 69–70. We understand Petitioner's contention to be that, when there are more than two channels and memory devices on two channels act together by "transfer[ring] information simultaneously" (Ex. 1071, 21:16–20), then the data accessed in a transaction would equal the bit width of the rank (devices on the two acting channels). *See* Pet. 70–72.

Patent Owner also argues that, "although much of the Petition's theory relies on the module width being 64 bits, the data width in Perego's Figure 4B is 16 bits." Prelim. Resp. 41. Even assuming Patent Owner is correct about Figure 4B, Perego expressly discloses a 64-bit wide embodiment, as discussed above. Ex. 1071, 14:12–15; Pet. 67.

Patent Owner also argues that "Perego's modules do not have a fixed width," which Patent Owner suggests runs counter to JEDEC compliant memories. Prelim. Resp. 34–35 (citing Ex. 2003, 43:12–20); *see also* Prelim. Resp. 36 ("Nothing in the '417 patent or any JEDEC documents suggests, however, a rank of memory devices refers to a group of memory devices that is dynamically reconstituted to account for the changing memory bit width."). Patent Owner, however, does not set forth a construction of "rank" that excludes such dynamic reconfigurability. On this record, it is not clear how a device that can have many configurations, one of which satisfies the limitations of a claim, would not render obvious the subject matter of that claim merely because it is capable of additional configurations.

Patent Owner also argues that Perego's disclosure in column 15 at lines 37–45 does not teach arranging memory in ranks. Prelim. Resp. 22–23 (citing Pet. 55). For the reasons discussed above in this section, we are sufficiently persuaded that Perego teaches ranks of memory devices by its disclosures of memories that act together to read or write, which are consistent with "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." Ex. 1071, 15:37–45.

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

h) Chip Select Signals Received by Memory Devices

Claim 1 recites "wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices [in] one respective N-bit wide rank of the plurality of N-bit-wide ranks."

Petitioner argues that chip select signals would have been received by memory devices consistent with JEDEC standards. Pet. 73–74 (citing Ex. 1064, 6; Ex. 1069, 2–3; Ex. 1003 ¶¶ 297–301); *see* Ex. 1064, 6 ("Package Pinout" table showing input for Chip Select).

Patent Owner cites the following disclosure from Perego: "According to embodiments of the present invention, subsets of available memory devices on configurable width buffered module 395 are activated or powered-on during various modes of operation. Thus, configurable width buffered module 395 is able to achieve power savings by only powering particular memory devices." Ex. 1071, 20:41–46, *quoted in* Prelim. Resp. 32. Patent Owner argues that, "[i]f the non-targeted ones are not even powered on, no registered signals could be received by them." Prelim. Resp. 32. We agree with Patent Owner that, if a device does not have power, it would not operate to receive signals, but Perego does not state that every embodiment operates like this. For its part, Petitioner relies on Perego's disclosure of devices being in a "ready or standby state" to support its contention that it would have been obvious to send a non-active chip select signal to those devices. *See* Pet. 59–60 (quoting Ex. 1071, 21:16–20; citing Ex. 1071, 15:40–45). On this record, we do not understand a "ready or standby state" to be a state in which no power is supplied to the memory device. Patent Owner argues that in such a state, "no commands are sent to

the non-targeted memory devices" (Prelim. Resp. 32), but Petitioner's combination is based on chip select signals as disclosed in JESD79-2 in combination with Perego's teachings of targeting only select memories.

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

i) Receive or Output Data in Response to Memory Commands

Claim 1 recites

> wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command.

Petitioner argues that Perego teaches this subject matter because it discloses reading from or writing to a target subset of devices (rank) while other devices remain in a standby state such that they are not selected as the target devices. Pet. 74–79 (citing Ex. 1071, 6:21–22, 11:56–61, 15:31–45, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 302–323). For example, Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more independent banks)" and "rout[ing] data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer)." Ex. 1071, 15:42–45, 11:56–61. Perego also discloses that "two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." Ex. 1071, 21:16–20.

Apart from its arguments about "ranks," discussed above in § II.E.2.g, Patent Owner does not dispute Petitioner's contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner's contentions and evidence that are summarized above, and we need not address Petitioner's additional arguments based on alternative claim constructions. *See* Pet. 81–84.

j) Circuitry

Claim 1 recites

> circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;
>
> wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

Petitioner argues that Perego discloses circuitry in the buffer devices of Figures 5A and 5B that is coupled between the data signal lines in the memory bus and corresponding data pins of memory devices in each of the ranks. Pet. 85–88 (citing Ex. 1071, 4:38–42, 6:12–15, 7:30–34, 10:59–67, 11:1–7, 13:6–10, 13:18–24, 14:65–15:2, 17:61–63, 18:65–19:3, Figs. 5A, 5B, 5C; Ex. 1003 ¶¶ 324–333). Petitioner argues that Perego's data bursts are routed through the buffer device between the targeted rank of memory and the memory controller and that a person of ordinary skill in the art would have understood that buffer control signals are used "to activate only the channel transferring the data burst between the memory controller and the targeted rank" and "to selectively activate those circuit elements of the buffer according to the targeted rank and direction of the read and write

operations." Pet. 90–91 (citing Ex. 1071, 6:15–25, 11:56–61, 12:9–12, 13:54–59, 14:62–15:6, 15:34–40, 17:41–44, 17:61–62, 21:16–20, Figs. 5A, 5B; Ex. 1003 ¶¶ 338–342).

As to the "CAS latency" recitations, Petitioner argues that the data are transferred according to an overall CAS latency of the memory module, citing Perego's disclosure of "access latency values" and JESD79-2's disclosure of CAS latency values. Pet. 92–94 (citing Ex. 1071, 12:20–34, Fig. 5B; Ex. 1064, 12, 14, 26, 28, Fig. 26; Ex. 1062, 68 n.1; Ex. 1003 ¶¶ 344–353). Petitioner argues that the data transfers in Perego are registered using latches 597f–m in Figure 5C. Pet. 95–96 (citing Ex. 1071, 12:65–13:5, 17:61–63, 18:65–19:3, Figs. 5B–5C; Ex. 1003 ¶¶ 359–362). Petitioner also argues that, "[u]nder the JEDEC standards, 'an additional clock cycle' is added to the 'CAS latency' of the memory devices to leave enough time for the register on the memory module to perform its functions." Pet. 95 (citing Ex. 1062, 68 n.1; Ex. 1064, 12, 14; Ex. 1003 ¶¶ 359–362). Petitioner argues that it would have been obvious to a person of ordinary skill in the art to add an additional clock cycle in Perego "so that the memory module complies with the timing of the JEDEC standards, and so the '*circuitry*' has enough time to perform its functions (including '*register[ing]*' the data signals for interfaces 520a/b with latches 597f-m . . .) using 'internal' clock circuit 570a-b." Pet. 95 (brackets by Petitioner; citing Ex. 1071, 12:65–13:5, 17:61–63, 18:65–19:3, Figs. 5B–5C; Ex. 1003 ¶¶ 359–362).

Patent Owner disputes Petitioner's contentions for the CAS latency recitations. Prelim. Resp. 42–45. As an initial matter, for the reasons explained above in § II.E.2, we disagree with Patent Owner's argument that

a person of ordinary skill in the art would not have combined the teachings of Perego and JESD79-2. *See* Prelim. Resp. 42.

Patent Owner argues that "Perego does not state that the 'access latency values' relate to the 'overall CAS latency of the memory module,' as opposed to a latency value of the memory device itself." Prelim. Resp. 43. The relied-upon portion of Perego discloses that "serial interface 574 may be employed to couple signals utilized in initialization of *module or memory device* identification values, test function, set/reset, access latency values." Ex. 1071, 12:20–24 (emphasis added). Thus, this disclosure suggests that the access latency values may pertain to the module and memory devices on the module. *See* Ex. 1003 ¶ 346 ("Perego discloses a serial interface 574 and operation circuit 572 including a ROM . . . that, during initialization of the module, provide identification information about the module, including 'access latency values,' that are used by the controller 'to properly configure the memory devices upon boot of the system.'" (citing Ex. 1071, 12:20–34)). Based on this evidence, we are sufficiently persuaded that Perego teaches access latency values for the memory module.

Patent Owner also argues that "Petitioner has also not provided competent evidence" to show that "the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices," as recited in claim 1. Prelim. Resp. 44. We disagree. Petitioner presents detailed testimony from Dr. Wolfe explaining how Perego's registered data transfers would have introduced delay. In particular, Dr. Wolfe, citing Perego's disclosures of data latches and an internal clock to generate synchronizing clock signals (Ex. 1071, 12:65–13:5, 17:61–63, Fig. C), provides the following testimony:

> A Skilled Artisan would have understood from these disclosures that Perego's latching of the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer because the output of the latch needs to be in synchronization with an internal clock. A Skilled Artisan would have understood that such registering of the data signals would require the addition of a fixed time delay, such as one clock cycle, for each registered data transfer through the circuitry with respect to the actual operational CAS latency of each of the plurality of memory integrated circuits.

Ex. 1003 ¶ 360. Dr. Wolfe further explains how Perego's "latching delays in the buffer device of Perego increase the overall CAS latency of the memory module compared to the CAS latency of the memory devices." Ex. 1003 ¶ 362 (citing Ex. 1071, 12:65–13:5, 18:65–19:3, Figs. 5B, 5C). On this record, we find Petitioner's evidence sufficiently persuasive to show that Perego teaches that "data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices," as recited in claim 1.

We are sufficiently persuaded by Petitioner's contentions for the remainder of the "circuitry" limitation, which we summarize above and which Patent Owner does not dispute at this stage. Having determined that Petitioner presents sufficiently persuasive evidence for this subject matter, we address Patent Owner's remaining arguments regarding this subject matter.

Patent Owner argues that "Petitioner ignores that Perego's buffer device includes caches that speed up data access." Prelim. Resp. 44 (citing Ex. 1071, 12:4–9). Perego, however, indicates that such a cache is optional ("may be incorporated"). Ex. 1071, 12:4–5. Even if a cache were

incorporated, its purpose is to store the "most frequently referenced data" so that they do not have to be retrieved from memory devices, which can speed up the memory module because the cache has "lower access latency characteristics than those of the memory devices." Ex. 1071, 12:5–9. This disclosure does not speak to the latched data that are otherwise retrieved from the memory devices when such data are not present in the cache.

Patent Owner also argues that Petitioner's reliance on Additive Latency (AL) in JESD79-2 falls short because "the actual operational CAS latency of a memory device would include the AL as well as specified" CAS latency. Prelim. Resp. 45 (citing Ex. 1064, 24; Ex. 1075, 15:52–57). Thus, according to Patent Owner, the CAS latency of the memory module would equal the actual operational CAS latency of the memory device, rather than being greater than the actual operational CAS latency, as recited in claim 1. Prelim. Resp. 45. We encourage the parties to address this argument further during trial because, to the extent the JESD79-2's disclosure of AL is specific to the memory devices themselves, it would appear that this AL would impact the actual operational CAS latency of the memory device. In any case, Petitioner presents evidence that a person of ordinary skill in the art would have taken into account the latency of the entire module, including latency of the memory devices combined with latency of the buffer device. Pet. 94 (citing Ex. 1003 ¶¶ 350–351; Ex. 1062, 68 n.1). This evidence sufficiently supports Petitioner's contentions.

Patent Owner also argues that Petitioner's reliance on the DDR RDIMM specification's disclosure of adding an extra clock cycle on the memory module is misplaced because (1) "Perego expressly distinguishes its data buffer to that on a traditional RDIMM" and (2) "no similar language is found in JEDEC's DDR2 RDIMM specification." Prelim. Resp. 43 (citing

Ex. 1071, 6:27–33; Ex. 1066, 94–96; Ex. 1062, 68). As to Patent Owner's first argument, we disagree for the reasons given above in § II.E.2.d based on Perego's disclosure of wanting to maintain backward compatibility. Ex. 1071, 2:4–6, 6:27–33, 6:37–39. As to Patent Owner's second argument, some additional development of the record would be helpful during trial.

We further note that claim 1's recitation that "data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" appears to pertain to the recited "circuitry," which is "*configurable* to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module" (emphasis added). The claim, therefore, appears to require a device that is configur*able* to perform data transfers in a certain way, rather than a device that is necessarily configur*ed* to do so. Based on the evidence presented, it appears that Perego's device has such configurability. In particular, Perego discloses the following:

> According to an embodiment of the present invention, clock circuit 570a–b includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock (not shown). Clock alignment circuit may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronizing clock signals having a predetermined temporal relationship.

Ex. 1071, 12:65–13:5. Dr. Wolfe's testimony indicates that this allows Perego to "add[] a predetermined amount of time delay for each data

transfer." Ex. 1003 ¶ 360. Thus, it appears on this record that Perego discloses the configurability recited in claim 1.

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner's contentions for the circuitry limitation.

k) Determination for Claim 1

For the reasons discussed above and based on Petitioner's contentions and evidence, summarized above, we are persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claim 1 is unpatentable as obvious over the combined teachings of Perego and JESD79-2. We note that Petitioner presents a short discussion of alleged secondary considerations of obviousness. Pet. 126–27. At this stage, Patent Owner does not present evidence of secondary considerations as to any of the challenged claims. Because we are sufficiently persuaded by Petitioner's showing, we need not rely on Petitioner's assertions of secondary considerations.

3. Claims 2–15

Petitioner also asserts that dependent claims 2–15 are unpatentable as obvious over the combined teachings of Perego and JESD79-2. Pet. 97–111. Patent Owner relies on the arguments addressed above in § II.E.2 and does not set forth additional arguments for claims 2–15 at this stage of the proceeding. *See* Prelim. Resp. 13–46. We have reviewed Petitioner's contentions, and we are sufficiently persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claims 2–15 are unpatentable as obvious over the combined teachings of Perego and JESD79-2.

F. Additional Grounds

As noted above, Petitioner asserts two additional grounds, each adding either Ellsberry or Halbert to the combination of Perego and JESD79-2 discussed above. Pet. 5, 111–26. Patent Owner opposes. Prelim. Resp. 45–59. Having determined that the Petition meets the threshold for institution (reasonable likelihood of prevailing as to at least one of the challenged claims) based on the Perego and JESD79-2 obviousness ground, the remainder of this Decision focuses on the parties' disputes to provide guidance to the parties for the trial.

1. Prior Art Status of Ellsberry

In an *inter partes* review, a petitioner "may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications." 35 U.S.C. § 311(b). Patent Owner argues that "patent applications are 'printed publication' prior art only as of the date they became published and available to the public." Prelim. Resp. 48. Patent Owner argues, therefore, that Ellsberry is not a prior art printed publication under 35 U.S.C. § 311(b) because it was published in December 2006, which is after the effective filing date of July 1, 2005, that Petitioner asserts applies to the '417 patent. Prelim. Resp. 46; *see* Pet. 5–6 (asserting that the claims of the '417 patent are not entitled to the benefit of a filing date before July 1, 2005).

We disagree with Patent Owner's statutory interpretation. Ellsberry is a printed publication, having been published in December 2006, as Patent Owner acknowledges. *See* Ex. 1073, code (43) (publication date of Dec. 7, 2006); *see also* Prelim. Resp. 47 (acknowledging publication date). On this record, we are persuaded by Petitioner's contentions that Ellsberry is prior

art under 35 U.S.C. § 102(e), having been filed "by another . . . in the United States before the invention by the applicant for patent." *See* Pet. 5–8 (asserting a priority date of no earlier than July 1, 2005, for the '417 patent); *see also* Ex. 1073, code (22) (filing date of June 1, 2005). Thus, Petitioner asserts a permissible ground of unpatentability under 35 U.S.C. § 311(b) by arguing that claims 1–15 are unpatentable under 35 U.S.C. § 103(a) on the basis of Ellsberry, which is a prior art printed publication, in combination with other prior art.

2. Combination of Perego, JESD79-2, and Ellsberry

Patent Owner also argues that "Ellsberry does not cure the deficiency of Perego," disputing various assertions of Petitioner as to Ellsberry's disclosure. Prelim. Resp. 48–54 (emphasis omitted). For the reasons discussed in § II.E.2, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches the subject matter of claim 1, and, therefore, on this record we do not agree with Patent Owner that there are deficiencies in the asserted combination.

With respect to Petitioner's reasoning to combine based on Ellsberry's disclosure of JEDEC compliance and DDR2 memories (Pet. 113–114), Patent Owner argues that "Petitioner does not explain why a [person of ordinary skill in the art] would modify Perego to make it comply with JEDEC." Prelim. Resp. 54. For the reasons explained above in § II.E.2, we disagree with Patent Owner.

3. Combination of Perego, JESD79-2, and Halbert

Patent Owner argues that "Halbert does not cure the deficiencies of Perego," disputing various assertions of Petitioner as to Halbert's disclosure. Prelim. Resp. 55–57. For the reasons discussed in § II.E.2, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches

the subject matter of claim 1, and, therefore, on this record we do not agree with Patent Owner that there are deficiencies in the asserted combination.

With respect to the CAS latency recitations of claim 1, Patent Owner argues the following:

> Petitioner has not pointed to any evidence that Halbert's data buffer is configured to transfer data in accordance with the overall CAS latency of the memory module, as opposed to the latency of the device after the device receives the read/write commands. Pet. 125–126. What the Petition at most shows is that due to the one-cycle delay between when the command is issued by the memory controller and when the device receives the command, the time interval between when the memory controller issues a read command and when data appears on memory bus is greater than the time interval between when the memory device receives the command and when data appears on memory bus. But that result does not evidence how the result is achieved: that is, the timing could simply result when the data buffer just transports data without reference to the overall CAS latency of memory module at all, but in reference to some other signals or parameters (e.g., the relevant data data strobe signals).

Prelim. Resp. 56–57 (citing Ex. 1078, 6:19–28).

As an initial matter, Patent Owner's argument does not appear to be commensurate in scope with the claim, which recites circuitry that is "configurable" to transfer data in a certain manner, not "configured" to do so. *See* § II.E.2.j above. Furthermore, it is unclear why Halbert's disclosure would not teach the CAS latency subject matter even if "some other signals or parameters" (Prelim. Resp. 57) cause the recited latency. In any event, we need not rely on Halbert at this stage because, for the reasons discussed above in § II.E.2.j, we are sufficiently persuaded by Petitioner's contentions based on Perego in combination with JESD79-2 for this subject matter.

Patent Owner also argues that Petitioner has not provided sufficient reasoning to combine Halbert with Perego and JESD79-2 and that Petitioner

"provides no detail whatsoever on how it suggests a [person of ordinary skill in the art] should incorporate Halbert's design in Perego." Prelim. Resp. 57–59. For claim 1, we understand Petitioner to be relying on "Halbert's disclosure of m-bit wide ranks . . . where 'm' can be 64 bits" to bolster its contention that having multiple ranks would have been obvious. Pet. 123–24. We also understand Petitioner to be relying on Halbert's disclosure of a memory module CAS latency that exceeds the CAS latency of a memory device on the module. Pet. 124–26. This latter teaching appears particularly relevant given the Examiner's reasons for allowance, which we discuss above in § II.A.2. *See* Ex. 1002, 229–30 (Examiner's reasons for allowance stating that the "closest prior art of record" does not teach the "circuitry" limitation, including the CAS latency recitations). On this record, we are sufficiently persuaded by Petitioner's reasoning that a person of ordinary skill in the art "would have recognized that the combination would have resulted in a predictable variation, which would improve similar devices like Perego in the same way and not yield unexpected results or challenges." *See* Pet. 122 (citing Ex. 1003 ¶ 198).

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging at least one claim of the '417 patent, and we institute *inter partes* review of all challenged claims on all grounds raised in the Petition. *See* 37 C.F.R. 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."). At this stage of the proceeding, we have not made a final

determination with respect to the patentability of any of the challenged claims or the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted as to claims 1–15 of the '417 patent on all challenges raised in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which will commence on the entry date of this decision.

IPR2023-00454
Patent 11,093,417 B2

FOR PETITIONER:

Eliot Williams
Theodore Chandler
Ferenc Pazmandi
John Gaustad
Brianna Potter
BAKER BOTTS LLP
eliot.williams@bakerbotts.com
ted.chandler@bakerbotts.com
ferenc.pazmandi@bakerbotts.com
john.gaustad@bakerbotts.com
brianna.potter@bakerbotts.com

FOR PATENT OWNER:

Hong Zhong
Jonathan Lindsay
IRELL & MANELLA LLP
hzhong@irell.com
jlindsay@irell.com